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# ANALYSIS OF POWER FACTOR AND HARMONICS IN POWER FACTOR CORRECTION TOPOLOGIES

Puthireddy Umapathi Reddy[1], Madithati Lakshmikantha Reddy[2],
Sirigiri Sivanagaraju[3]
[1,2]Department of Electrical and Electronics Engineering,
Sree Vidyanikethan Engineering College, Tirupati-517102, India.
[3]Department of Electrical and Electronics Engineering, Jawaharlal Nehru Technological University College of Engineering Kakinada, Kakinada-533 003, India.

***ABSTRACT***
*The analysis is based on the fact that virtually all power factor correction (PFC) converters use a few basic converter topologies as their input stages. It is found that these converters present distinctive harmonic behaviors. Harmonic current contents and the resulting power factors that are associated with these converters under different conversion ratios are obtained analytically. A switch-mode dc-to-ac inverter based on a dc-to-dc converter topology using a novel nonlinear robust control to generate a sinusoidal output waveform is simulated. The control scheme is such that the output voltage remains dynamically unchanged when there are large disturbances in input voltage or load current. Computer simulation result shows the robustness and fast dynamic response of the control system. This type of inverter has many advantages over the traditional bridge-type inverter. The stability analysis of the control system and MATLAB simulation results are provided. The ultimate objective of this paper is simulation of a switch-mode inverter with dc-to-dc converter topology, which employs a nonlinear robust control strategy so as to acquire the a good steady state and dynamic performance. Output voltage remains dynamically stable when the supply voltage or load current suddenly changes (zero voltage regulation).*

***KEYWORDS:*** *Power factor, Harmonics analysis, Correction topologies, MATLAB simulation.*

## I. INTRODUCTION

DC-to-DC power converters converts electrical power provided from a source at a certain dc voltage to electrical power available at different dc voltages. Dc-to-dc power converters form a subset of electrical power converter [1]-[3]. Both the input and output power specifications of the dc to dc power converter are in dc .most of the dc loads require a well stabilized dc voltage capable of supplying a range of required current or a variable dc current or pulsating dc current rich in harmonics[4],[6]. The dc to dc converter has to provide a stable dc voltage with low output impedance over a wide frequency range. These features of the dc-to-dc converter are known through the output regulation and output impedance of the converter. The dc-to-dc converter must maintain the integrity of the output power in the presence of these non-idle sources characteristics [5]. This capability of dc-to-dc converter is known through the line regulation, ripple susceptibility and the input impedance of the converter. Power system harmonic issues arise from large number of nonlinear loads that are present in the power systems [7]-[8]. Harmonic currents degrade power quality and are considered the main source of many system malfunctions [12]. This problem attracted increasing concerns in the

recent past and several technical guidelines regarding suppressions of system harmonic contents have been enacted [9]-[11]. In low and medium power applications, active power factor correction (PFC) converters have been a constant topic in recent years [13]-[15]. In [17-19] Power Factor is described as leading for capacitive loads (i.e., current builds up faster than voltage) and lagging for inductive loads (i.e., current builds up slower than voltage). In both these circumstances, the power provided by the utility with less than that which is indicated by a simple multiplication of Volts times Amps. As, among other things, this situation compromises normal conductor sizing algorithms, utility companies often place limits on acceptable power factors for loads (for example <0.8 leading and >0.75 lagging)[16]. Financial penalty charges will often be imposed on loads that violate these requirements [19].

In this paper the power factor and harmonic levels of the basic power factor correction circuits operating on discontinuous current mode (DCM) are analyzed and evaluated according to different conditions followed by theoretical analysis and MATLAB results are shown to analyze stability analysis.

## II. SIMPLE DC-TO-DC CONVERTER

The simplest and traditional dc-dc converter is shown in figure 1.

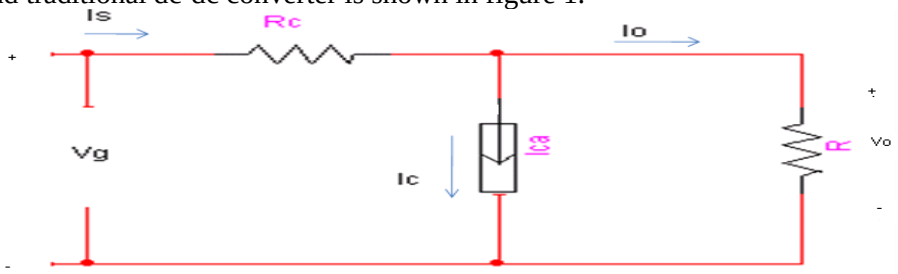


**Figure 1**. Simple dc-dc converter

Power is available from a voltage source of Vg. The load connected to the output of the converter is resistive (R) demanding power at a voltage level of Vo (Vo <Vg). The output voltage of the converter may be readily found as a function of Rc, Ic, Vg and R[6].

$$Vo = \frac{(Vg - IcRc)R}{R+Rc} \qquad (1)$$

## III. POWER FACTOR AND HARMONIC CURRENT DISTORTION OF BASIC PFC CIRCUITS

In these circuits the inductor (l) is the main energy transfer element and the inductor current has always been discharged to zero at the beginning of each switching cycle. Large storage elements are required to compensate for the inequality in between the instantaneous input and output power [2]. In many applications, the output capacitor of the buck, boost, buck-boost converters can be used for this purpose when these converters are utilized as the front-end PFC circuits. In the following analysis, it should be understood that voltage vo is the equivalent voltage across the storage capacitors that is responsible for discharging the inductor current [8]. Also R represents the loading effects of the output dc-to-dc stage.

To achieve high quality input characteristics for PFC circuits operating in DCM condition, the average line current within each switching cycle should follow closely the line voltage. The main power switch is turned on for a fixed time in each switching period. This time is determined by the control circuit such as desired amount of power can be transferred to the output. This often results in satisfactory power factor in many designs. For buck-boost PFC circuit and its variations, an exact sinusoidal input current can even be obtained after high frequency components are filtered out [12]. However, for buck and boost PFC circuits, harmonic currents are present in the input current and they are dependent on circuit operation conditions. These relations are revealed analytically. In the following analysis, assumed that the duty cycle is represented as ‘α’ is constant.

### 3.1 Buck Pfc Circuit

The circuit topology and its input current (or rectified line current) waveform in a switching period is given in [4] Assume $V_{line}$ (t) =$\sqrt{2}V_{in}$sinωlt , where $V_{in}$ and ω1 are the rms value of the line voltage and line fundamental angular frequency, respectively. The average input current over a switching period Ts, could be obtained [10]:

$$i_{line,avg}(t) = \frac{\alpha^2 T_s}{2L}\left(\sqrt{2}V_{in}\sin\omega_1 t - V_o\right)$$
$$= \frac{\alpha^2 T_s}{2L}V_{in}\left(\sqrt{2}\sin\omega_1 t - M\right) \quad (2)$$
$$= \frac{\alpha^2 T_s}{2L}V_{in}\sum_{n=1}^{\infty}\left(a_n\cos n\omega_1 t + b_n\sin n\omega_1 t\right)$$

Where an and $b_n$ are the fourier series coefficients. M is the voltage conversion ratio and is defined as:

$$M = \frac{Vo}{Vin} \quad (3)$$

Proper operation of the buck converter requires that m<√2. Also, rectifier bridge does not allow nonzero input current input current when |vline (t)| < vo. Because of the symmetrical property of the average input current waveform, the fourier series coefficients are obtained as:
$a_n$=0, n=1,2,3,...
$b_n$=0, n=2,4,6,.

$$b_1 = \frac{\sqrt{2}}{\pi}\left(\pi - 2\theta - M\sqrt{2-M^2}\right) \quad (4)$$

$$b_n = \frac{2\sqrt{2}}{\pi}\left(\frac{\sin(n+1)\theta}{n+1} - \frac{\sin(n-1)\theta}{n-1} - \frac{\sqrt{2}M\cos n\theta}{n}\right) \quad (5)$$

For n = 3, 5, 7, ……., , where $\theta = \sin^{-1}\frac{M}{\sqrt{2}}$

Total harmonic distortion factor of the input current thd and power factor of the pfc circuit pf can be calculated from eqs. (4) and (5) according to the following definitions:

$$THD_i = \sqrt{\sum_{n=2}^{\infty} I_n^2}\Big/ I_1 = \sqrt{\sum_{n=2}^{\infty} DFI_n^2} \quad (6)$$

$$pf = \frac{I_1\cos\phi}{I} = \frac{\cos\phi}{\sqrt{1+THD_i^2}} \quad (7)$$

Where i1,in and φ are fundamental, nth harmonic current (rms values) and phase shift between line voltage and fundamental current, respectively. $DFI_n$ is the nth harmonic current distortion factor. As the average input current always follows the voltage, it is obvious that cosφ=1 [2]. According to eqns.(6) and (7), it is clear that pf and $THD_i$ are only dependent on conversion ratio m.

### 3.2 Boost Pfc Circuit

The circuit topology of a boost converter and its input current waveform in a switching period is given in[6]. The average input current in each switching period is:

$$i_{line,avg}(t) = \frac{1}{T_s}\left[\frac{1}{2}(\alpha+\alpha_1)T_s\frac{V_{line}(t)}{L}\alpha T_s\right]$$
$$= \frac{\alpha^2 T_s V_o}{2L}\frac{\sqrt{2}\sin\omega_1 t}{M - \sqrt{2}\sin\omega_1 t} \quad (8)$$

$$= \frac{\alpha^2 T_s}{2L} V_{in} \sum_{n=1}^{\infty} \left( a_n \cos n\omega_1 t + b_n \sin n\omega_1 t \right)$$

In this equation, m is also the voltage conversion ratio as defined in eq.(3). Once again, it is required that m>√2 for proper operation of the PFC circuit. Equation (8) suggests that if m is much larger than 1.5, the average input current is much closer to a sinusoidal waveform; hence near unity power factor can be obtained. The symmetrical property of the current waveform also ensures that an=0, b2n=0 (n=1,2…….). Other fourier coefficients can be obtained as

A near unity power factor (>0.99) can easily be obtained with the boost circuit when m>3. The small distortion in the input current is caused by the existence of α1ts required to discharge the inductor current (6). The higher the output voltage , the faster the inductor current reduces to zero and therefore the average input current over a switching period is more closely proportional to the line voltage.

### 3.3 Buck-Boost Pfc Circuit

The circuit topology and input current waveform of the buck-boost circuit operating in DCM is shown in[6]. it can be noted that input current in each switching period is equal to the inductor current when the switch s is ON. Therefore average input current over a switching period can be calculated below:

$$i_{line,avg} = \frac{1}{T_s} \frac{1}{2} \alpha T_s \frac{V_{line}(t)}{L} \alpha T_s = \frac{\alpha^2 T_s V_{in}}{\sqrt{2}L} \sin \omega_1 t \qquad (9)$$

equation (9) shows that the buck-boost circuit would not introduce harmonic distortions to the line current and hence is perfect for PFC applications [2] . it also does not impose any limitation on the magnitude of the storage capacitor voltage. This excellent input property enables designers to have more freedom in choosing operation condition.

## IV. INVERTERS USING A DC-TO-DC CONVERTER TOPOLOGY

The dc-dc converters are widely used in regulated switch-mode dc power supplies. Often the input to these converters is an unregulated dc voltage, which is obtained by rectifying the line voltage, and therefore it will fluctuate due to changes in the voltage magnitude. switch-mode dc-to-dc converters are used to convert the unregulated dc input into a controlled dc output at a desired voltage level.

Recently, switch-mode dc-to-ac inverters using a dc-to-dc converter topology have been developed. Here a dc-dc converter and a controlled bridge (bridge synchronizer) are connected in series to realize an inverter. Using the dc-dc converter, controlled dc output in the form of a fully rectified sinusoidal wave is generated which becomes the input for the controlled bridge which then outputs a pure sine voltage waveform.

The principle of operation of this type of inverter is illustrated in [5], where the dc-to-dc converter is of buck configuration with the average output voltage of this buck converter (Vo) is the product of duty ratio and the input voltage i.e., if the input voltage is constant and the duty ratio is varied slowly, relative to the switching frequency, in the form of a fully rectified sinusoidal wave, the output will naturally be a fully rectified sine wave. Through a bridge circuit, which is synchronized with the fully rectified sine waveform of the duty ratio of the dc-dc converter, the output is "unfolded" into a sinusoidal waveform.

In this type of inverter both the magnitude and frequency of the output are controlled by the dc-dc converter, which depends on the magnitude and frequency of the reference signal. Several efforts have been made to improve the dynamic performance of this inverter, i.e., the output voltage remains dynamically unchanged when subjected to large disturbances in supply voltage or load current [7].

## V. STABILITY ANALYSIS

In fig 6.9 shows the root locus of the closed control system when the proportional gain of the error amplifier of feedback loop kp varies from $k_p = 1$ to $k_p = 100$. The control system is unstable for the given parameters because two roots are in the right half of the s-plane.

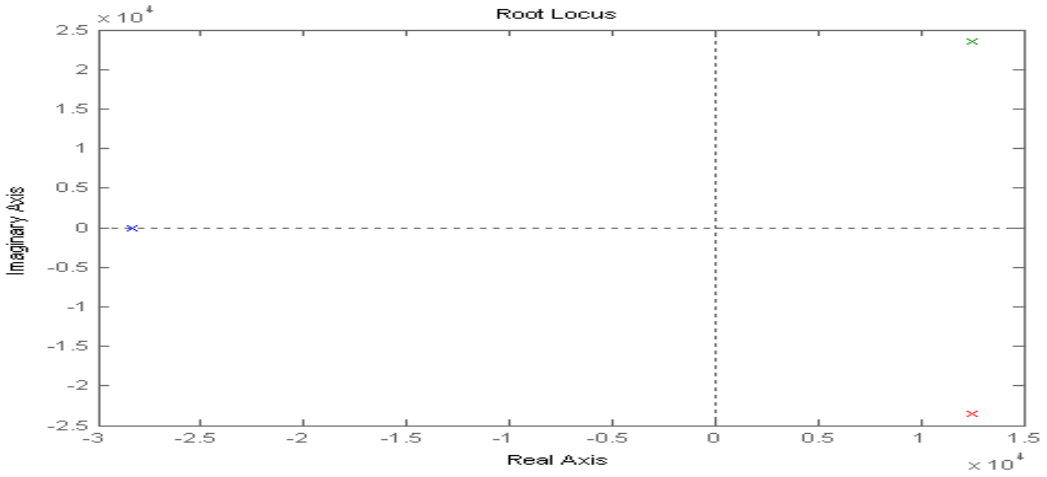


**Figure 2.** Root locus plot of the control system with P control (kp=1 to 100)

## 5.1 Proportional-Plus-Derivative Control

With similar steps shown in p controller the duty ratio generated by the control circuit with PD control of output voltage feedback loop is expressed as Root locus analysis is performed for the closed-loop control system with PD control. Figure 3.(a) and (b) gives the root loci of the closed-loop control system. The derivative gain $K_d$ is fixed at $K_d = 0.01$ and $K_d = 0.1$, respectively while the proportional gain $K_p$ is being varied from 1 to 100. All the roots are in the left half of s plane. For each value of $K_d$ there are three segments. One segment is on the real axis and becomes the dominant root and the other two segments are conjugate and lie far away left from the real root. Figure 3.(b) gives the root loci of the pd control for Kp=10 while the Kd is varied from 0 to 0.01.

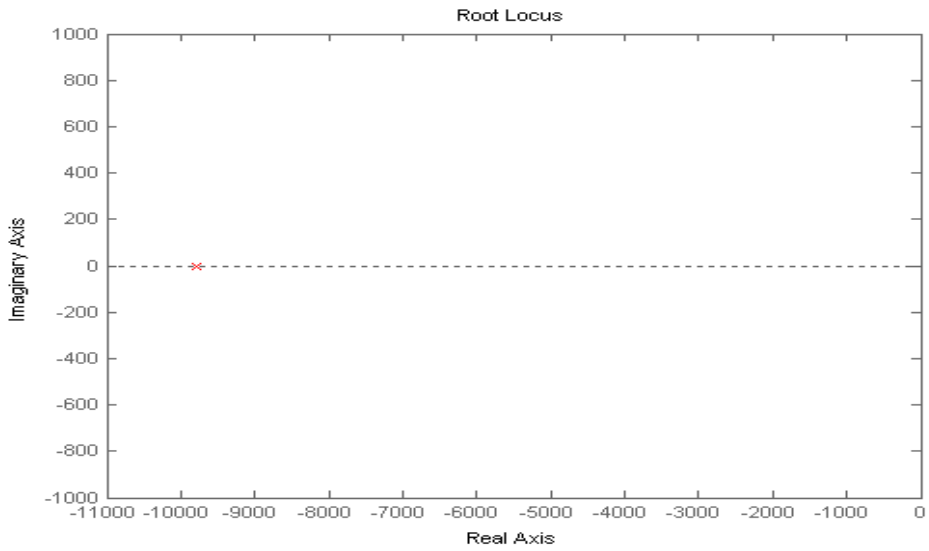


**Figure 3. (a).** Root locus plot of the control system with PD control (kp =1-100, kd=0.03)

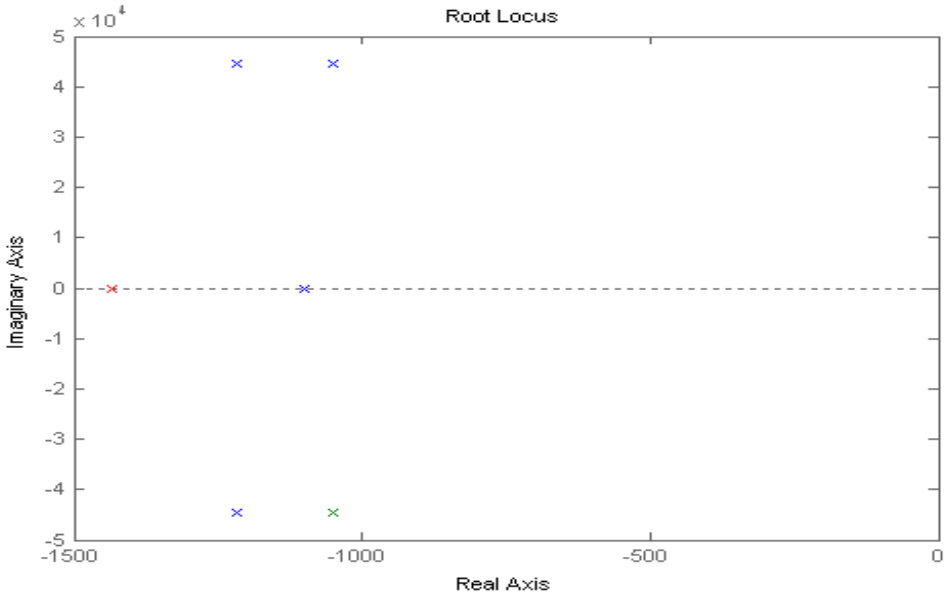


**Figure 3. (b).** Root locus plot of the control system with PD control (kp =10, kd=0-0.01)

It can be seen that as the $k_d$ value is increased, the two conjugate roots move into the left half of s-plane. Thus, from the analysis it is seen that for the given parameters, the system can be stabilized when the gain $K_d$ is proper.

## VI. RESULT ANALYSIS

The input characteristics of buck and boost converters are show in figure 4.: The parameters of the buck converter are input voltage $V_{in}$ = 110 V dc, Inductance l = 1mH, Switching frequency Fs= 50khz duty ratio=0.34.

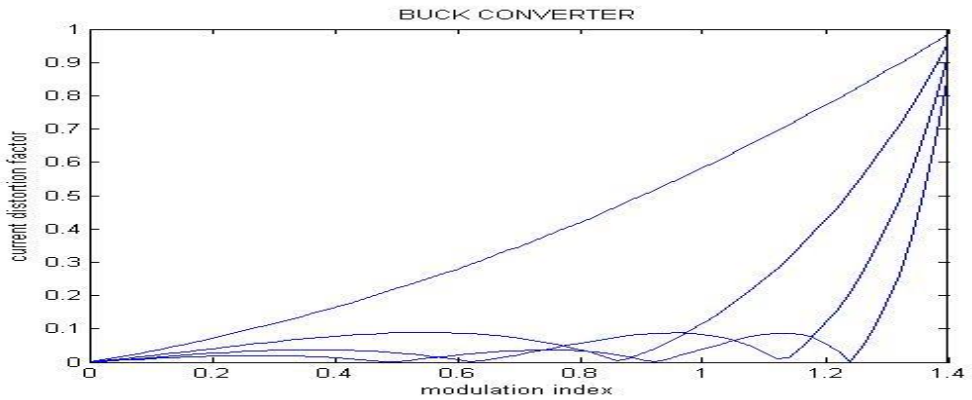


**Figure.4.** Harmonic current distortion factor of the buck converter vs. Conversion ratio

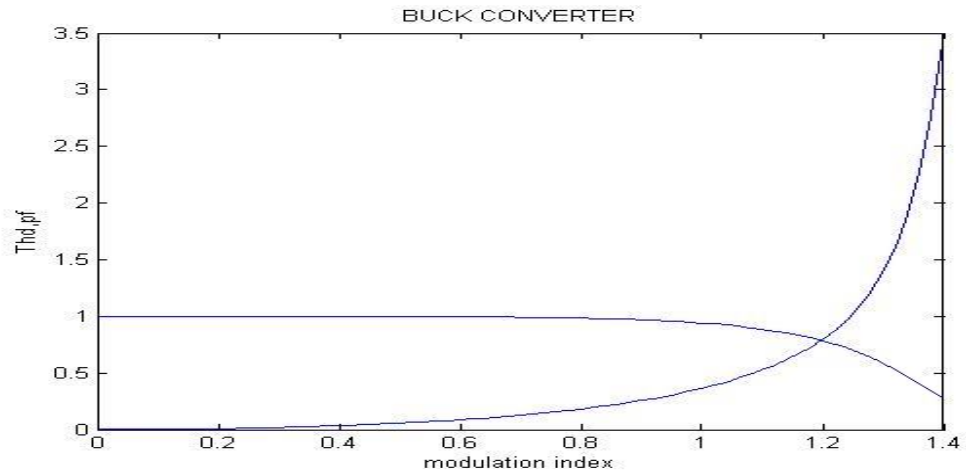


**Figure 5.** Power factor and total harmonic distortion of the buck converter vs. conversion ratio.

From the characteristics of buck converter, it is noted that

- The main harmonic component of the buck PFC circuit is the third harmonic current.
- As modulation index (M) increases, other harmonic components increase rapidly.
- Drastic distortion of the input current and poor power factor can be expected with large M, indicating that the buck converter is not a good circuit for DCM-PFC application where large storage capacitor voltage is present.

The parameters of the boost converter are as follows: Input voltage (Vin) = 110V dc, Inductance(l) = 1mH, Switching frequency(Fs) = 50kHz, Duty ratio(α)=0.34.

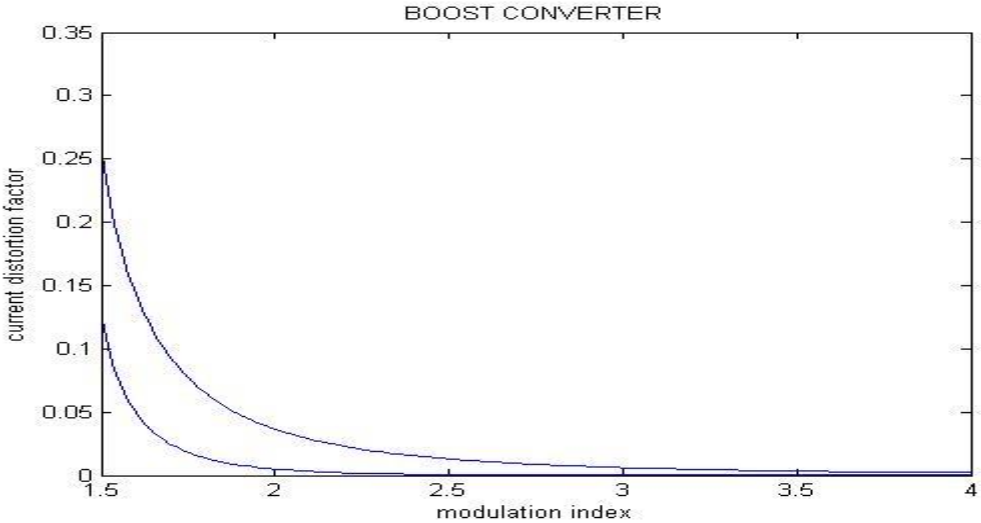


**Figure 6.** harmonic current distortion factor of the boost converter vs. conversion ratio.

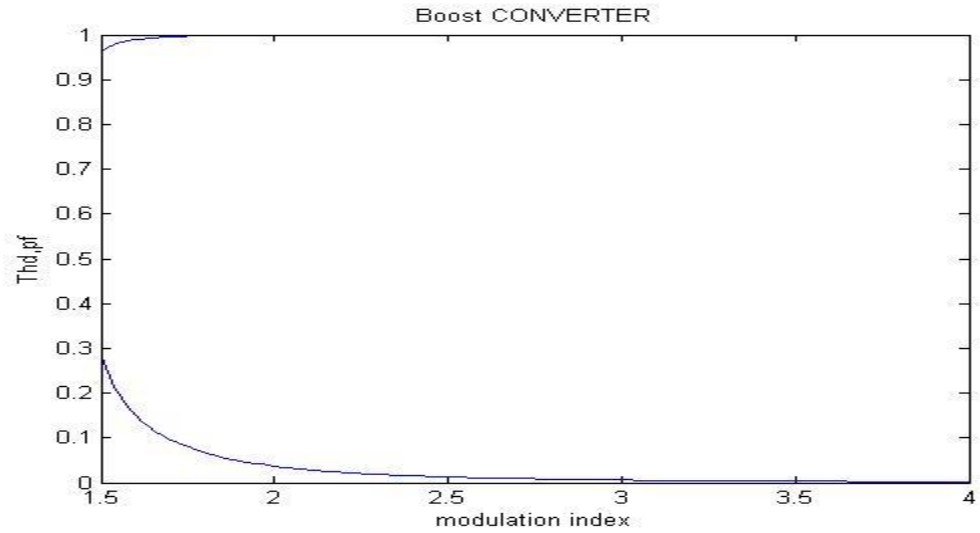


**figure 7.** power factor and total harmonic distortion of the boost converter vs. conversion ratio.

From the characteristics of buck converter, it is stated that, the harmonic distortion in the average input current for a boost circuit is much smaller than that of a buck circuit in PFC applications. On the other hand, achieving small input current distortion is at the expense of increasing voltage stress on the storage capacitor, thus requiring larger voltage rating capacitors.

## VII. CONCLUSIONS

Power factor and harmonic characteristics of three basic high frequency switched mode PFC circuits are obtained using MATLAB program. The results can facilitate PFC power supply designers in choosing appropriate circuit topologies and estimating the input characteristics of their design. The inverter with dc-to-dc converter topology has been simulated using MATLAB simulation. The simulation results conclude that the nonlinear robust control, which has been employed, provides dynamical stabilization of the output voltage of the inverter thus achieving zero voltage regulation. Also with dc-to -dc converter topology for the inverter pure sinusoidal output has been generated. Stability analysis of the control system under proportional and proportional derivative control of the output voltage feedback loop is carried out.

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## IX. AUTHORS

**P.UMAPATHI REDDY**: He received his B.E from Andra University, M.Tech.,(Electrical Power Systems) from Jawaharlal Nehru Technological University, Anantapur, and did his Ph.D. from Jawaharlal Nehru Technological University Kakinada, Kakinada, India in 1998 2004 and 2013 respectively, Currently he is working as a professor in the department of Electrical and Electronics Engineering, Sree Vidyanikethan Engineering College, Tirupati, India. His research interest includes Power Distribution Systems, Power System Operation and Control and Power electronic devices applications in power systems. He is life member of Indian Society for Technical Education and The Indian science Congress Association.

**M. Lakshmikantha Reddy**: He received his B.Tech., from JNTU University and M.Tech.,(Power Systems) from, NIT, Warangal, India in 2001 and 2005 respectively, Now he is pursuing Ph.D. degree. Currently he is with Department of Electrical and Electronics Engineering, Sree Vidyanikethan Engineering College, Tirupati, India. His research interest includes Power electronic devices applications in power systems and Power System operation and control. He is Member of The Indian Science Congress Association.

**S. Sivanaga Raju**: He received his B.E from Andra University and M.Tech. degree in 2000 from IIT, Kharagpur and did his Ph.D from Jawaharlal Nehru Technological University, Anantapur, India in 2004. He is presently working as professor in J.N.T.U. College of Engineering Kakinada,(Autonomous) Kakinada, Andra Pradesh, India. He received two national awards (Pandit Madan Mohan Malaviya memorial Prize and best paper prize award from the Institute of Engineers (India) for the year 2003-04. He is referee for IEEE journals. He has around 90 National and International journals in his credit. His research interest includes Power distribution Automation and Power System operation and control. He is life member of Indian Society for Technical Education.