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A SILICON LDMOS BASED RF POWER AMPLIFIER FOR WIRELESS BASE STATION APPLICATIONS

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ABSTRACT
Radio Frequency Power amplifier is one of the essential module in the transmission chain of wireless Base stations. There is always a trade-off exists between power efficiency and linearity of the power amplifier. The design of power amplifier using LDMOS based active devices will give cost-effective solution. This work presents the design of a Class A power amplifier for unlicensed ISM band wireless Base station requirements. The design is carried out using Si-LDMOS (Silicon - Laterally Diffused Metal Oxide Semiconductor) technology and is built on Epoxy-FR4 (Flame Retardant, woven glass reinforced epoxy resin) board with a dielectric constant of 4.6 and substrate thickness of 1.6 mm. The amplifier design uses Free scale Si-LDMOS MW6S004NT1 transistor model in Agilent's Advanced Design System (ADS 2011). The simulation was carried out to analyze the behaviour of power amplifier in the 2.4GHz ISM band. The simulated results has shown an acceptable behaviour with a gain of 16.558 dB, power added efficiency of 61.897% at 2.4 GHz, which allow the use of the device in the wireless base station application requirements.

KEYWORDS : *Si-LDMOS , Linearity, Power gain , Power added efficiency , Advanced design system Stability.*

I. INTRODUCTION

Until recently, WiMAX, WiFi, WLAN systems have used technology processes such as Gallium-Arsenide (GaAs) to obtain the performance needed from the RF circuits [1]. Although these technologies provide the functional performance required by radios today, they do not support the cost/scalability business model. But as the MOS technology is being developed, certainly with CMOS and LDMOS, more research is currently investigating the use of these technologies in radio frequency systems, such as in power amplifiers [2].
Analog solutions implemented in Si-LDMOS will achieve high performance, functionality, and bandwidth while maintaining low cost, high quality and robust architecture across the wireless market [3]. High gain and good linearity are among the very important characteristics of a base station power amplifier used in majority of the applications [4,5]. Till now power amplifiers have been designed to fulfil the demands of RF applications using Gallium-Arsenide (GaAs), but it comes at the expense of the cost. To solve this issue, current researches are investigating the possibility of using cheaper technologies such as Si-LDMOS in power amplifier implementation [6,7].

In this paper, the design of a power amplifier based on a Si-LDMOS transistor at 2.4 GHz relying on ISM band specifications is illustrated. The power amplifier is built on Epoxy-FR4 board with a dielectric constant of 4.6. Furthermore, all the simulations were done in ADS 2011 simulator in order to optimize the design and to study the performance. After getting the optimised power amplifier performance parameters, a layout implementation is followed.
The remaining sections of this paper are organised as follows. Section 2 describes the fundamental parameters to be considered for the power amplifier design. Section 3 illustrates the step by step power amplifier simulation sequences in ADS. Experimental results obtained from simulation are also discussed in section 3. Conclusion is given in Section 4.

II. POWER AMPLIFIER FUNDAMENTALS

One of the most important modules in a RF system chain is the power amplifier. In fact, at the transmitter side in a base station, a power amplifier is established to increase the signal power and allow longer distance transmission. The growth in wireless communications and radar applications has put greater demand on the performance of power amplifiers [8]. Choosing the bias point of an RF Power Amplifier can determine the level of performance. In certain applications, it may be desirable to have the transistor conducting for only a certain portion of the input signal. The comparison of PA bias approaches evaluate the trade offs for: Output Power, Efficiency, Linearity, or other parameters for different applications. In order to operate a transistor for a certain class, the gate and drain DC voltages have to be biased carefully to certain operation point (quiescent point or Q point), regarding the desired class. The reason is that the choice of Q-point greatly influences the linearity, power handling and efficiency. In addition, the choice of optimal Q point is limited by a safety region which prevents the transistor from being heated badly to damage.

There are several types of power amplifiers and they differ from each other in terms of their linearity, efficiency and power output capability. For example, communication systems which require good linearity often use Class A or Class AB architecture whereas those which require good efficiency use a Class C, E or F type power amplifier. The most important parameters that must be considered when designing power amplifiers are listed below [9,10].

2.1 Power

In RF and Microwave circuits, power has two understandings: the power available from the source and the power transferred to or dissipated in the load. Available power is the maximum power accessible from the source. The power dissipated in or transferred to the load is expressed by,

$$P_d(W) = \frac{V_L(W)}{2\,\mathrm{Re}\{Z_L(W)\}} \qquad (1)$$

where $V_L(w)$ is the peak value of the sinusoidal output voltage and Re {ZL(w)} is the real part of the load impedance.

2.2 Efficiency

Efficiency or drain efficiency is simply defined as the ratio of output power at the drain (PO) to the input power supplied to the drain by the dc supply (PDC).

$$\eta = \frac{P_0}{P_{DC}} \qquad (2)$$

2.3 Power added efficiency (PAE)

Power added efficiency (PAE) includes the effect of input drive power (P_{IN}) and is defined as,

$$PAE = \frac{P_0 - P_{IN}}{P_{DC}} \qquad (3)$$

2.4 Gain

It is the ratio between the power delivered to the load and the power available from the source. Transducer gain can be expressed by,

$$G = \frac{P_L}{P_S} \qquad (4)$$

where P_S is the RF input power and P_L is the RF output power.

2.5 Linearity

The RF power amplifiers are inherently non-linear and are the main contributors for distortion products in a transceiver chain. Non-linearity is typically caused due to the compression behaviour of the power amplifier, which occurs when the RF transistor operates in its saturation region due to a certain high input power level. Some of the widely used parameters for quantifying the linearity are 1 dB compression point, third order intermodulation distortion and third order intercept point (IP3).

2.6 Stability

Stability is a practical problem frequently encountered in the design of linear PA. The Rollet's conditions [11] are based on the two-port S-parameters matrix expressed as:

$$\Delta = \det(S) = S_{11}S_{22} - S_{12}S_{21} \qquad (5)$$

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} \qquad (6)$$

For unconditional stability: K > 1 and |Δ| <1, otherwise the stability has to be taken into account.

III. LDMOS Power Amplifier Design And Simulation

The model used in the current design is the Freescale Si-LDMOS MW6S004NT1 model. Designing a power amplifier consist of several steps. A DC simulation must be done to find the optimal bias point and bias network for the system. Then a small signal S-parameter simulation is done to find the value of the S-parameters and to evaluate the stability of the model over the frequency range. After that the input and output matching network are designed using load pull simulation. Finally the whole system is optimized to achieve better output power, efficiency and gain.

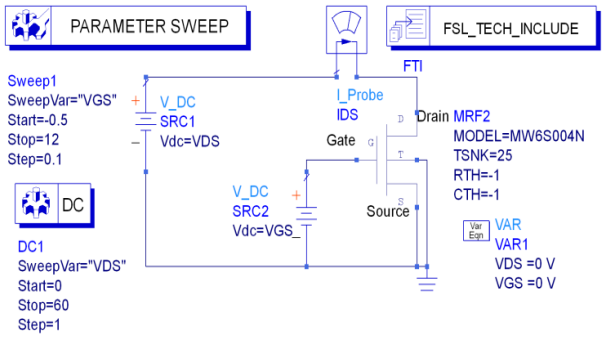

Figure 1. Schematic of DC simulation setup

3.1 DC Voltage Current Characteristics

The first step of design in this paper is to estimate the I-V curves. The I-V curves help to see, for example, the operation region of a transistor, threshold voltage and safety region etc. The DC simulation setup and LDMOS output characteristics are shown in Figure 1 and Figure 2. Load line curve is plotted from the output characteristics of the transistor. To operate the amplifier in class A mode center of the load line is selected for biasing. We selected the biasing voltages of VDS as 40V and VGS as 4V.

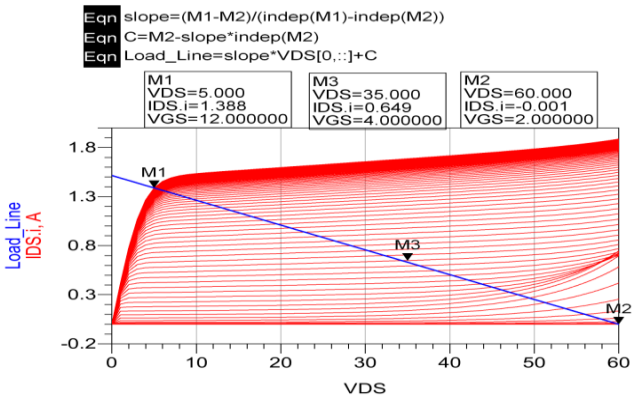

Figure 2. Load Line analysis of LDMOS output characteristics

3.2 Bias and Stability Analysis

A passive bias is used which consists of a block of capacitors and inductors. These blocks will behave as a DC feed-RF block in the DC trajectory. Their values are chosen regarding the range of frequency the system is supposed to work at 2.4 GHz. The PA system including the bias network is shown in Figure 3. The small-signal S-parameter simulation was performed in the design to find the value of the S parameters and the stability region of the biased transistor. In fact, as class A amplifiers present the highest linearity between the other types and despite the fact that we are designing a high power amplifier, the S-parameters are still usable certainly in designing the input matching network.

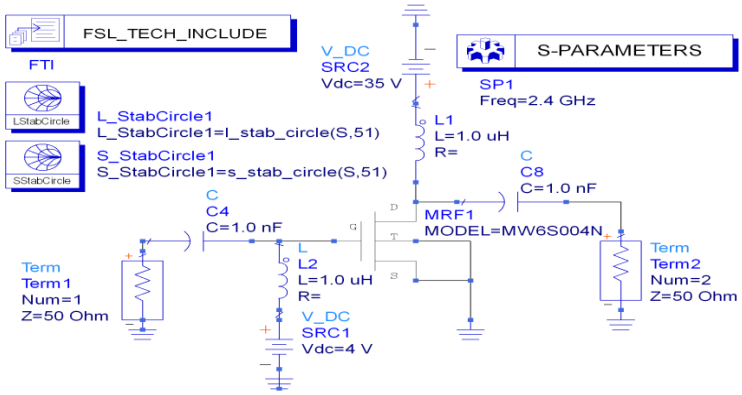

Figure 3. Bias and stability analysis

The results of the S-parameters simulation are
S11 = 0.934 ∠149.89º, S21 = 0.003 ∠-119.345º, S12 = 2.993 ∠-16.04º and
S22 = 0.806 ∠ -175.463º
From the S Parameters simulation results, the values of Δ and K are determined using equations (5) & (6).
Δ = 0.7439 < 1 and K= 1.754>1. This calculated values of Δ & K shows that the system is unconditionally stable for the selected biasing configuration.

3.3 Load pull simulation

Load pull simulation is performed to find the optimal load value that will maximize the output power and the efficiency or to achieve a compromise between both of them. The analysis utilizes the built-in ADS load-pull circuit simulator. Different values of load impedance are applied to find out the optimum one, which meets the required value of gain, output power and efficiency.

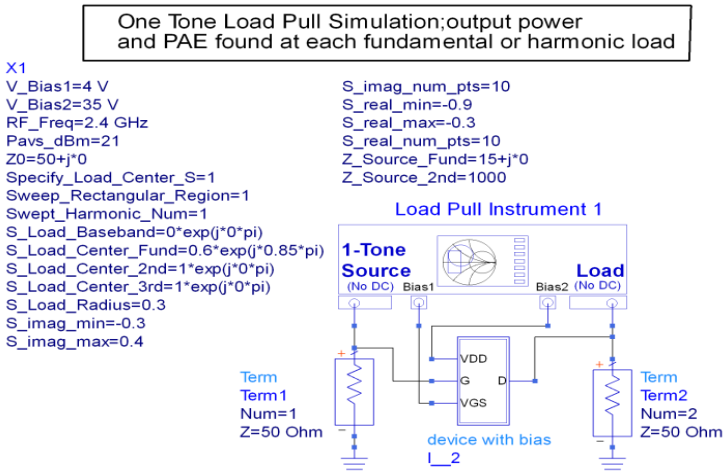

Figure 4. Load pull simulation setup

The derived value of the optimum load impedance is going to be used for designing a matching network. The simulation setup of load pull simulation is shown in Figure 4.The load pull simulation gave an optimal output power of 33.53 dBm, PAE of 61.8% for the input impedance of Zi = 4.933+ j*11.867 and output impedance of Z_L = 8.821+j 0.384 ohms.

3.4 Matching network design

The impedance values obtained from load pull simulation are used to design the matching networks. There are several ways to design the matching networks. The simplest technique is to use the lumped circuit elements. Another method is to use microstrip line either single-stub or double-stub matching technique. Lumped element realization of the matching network at high frequencies leads to parasitic and coupling effects [12]. Here, microstrip line method was chosen over the lumped circuit element matching method because of the ease of implementation of the actual circuit on the board.

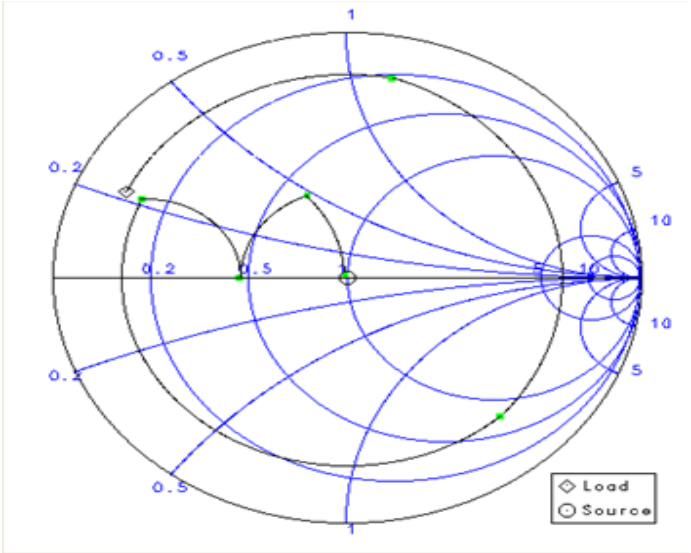

Figure 5. Input Matching design using Smith Chart

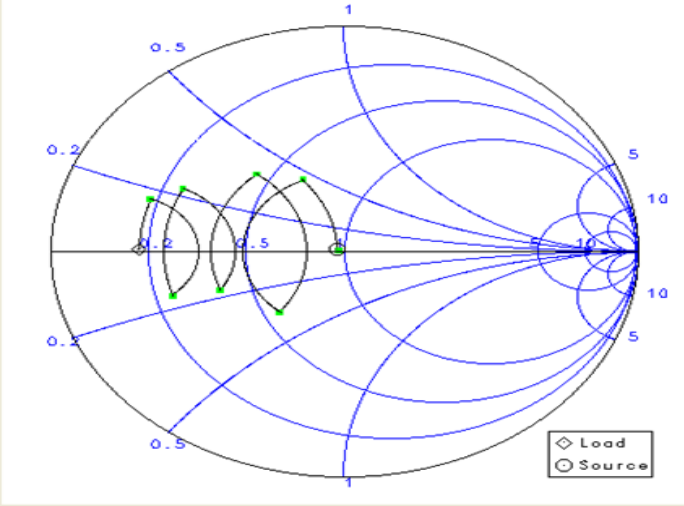

Figure 6. Output Matching design using Smith Chart

The matching network for the power amplifier has been designed using the Smith Chart tool in ADS, which provides greater control on the impedance matching network design. The input impedance obtained from load pull simulation is Zi = 4.933+ j*11.867. This impedance value has to be matched to a source impedance of 50Ω. The impedance transformation is obtained by using a sets of series and shunt configured transmission line sections. The transition from the input impedance of Zi to the centre of the smith chart for 50 Ω is shown in Figure 5. The series transmission lines are equallent of inductors and shunt configured lines are equallent of capacitors. The corresponding electrical lengths of the microstrip series and shunt stubs are illustrated in Table 1. The same procedure is followed to obtain the output matching network. The load impedance is 50 Ω which appears at the center of the smith chart. The amplifier output impedance of 8.821+ j0.384Ω is finally matched to the 50 Ω transmission line impedance by using series and shunt microstrip transmission lines. The smith chart aided output matching is shown in Figure 6. The microstrip nature of input and output matching networks are shown in Figure 7 & 8.

Table 1. Electrical length values of input and output matching sections

Section	Electrical Length			
	Input matching		Output matching	
	Series	Shunt	Series	Shunt
1	90	37.408	9.459	77.819
2	33.925	73.180	22.719	71.379
3	78.511	51.542	35.538	62.613
4	37.55	-	58.454	36.876
5	-	-	90	-

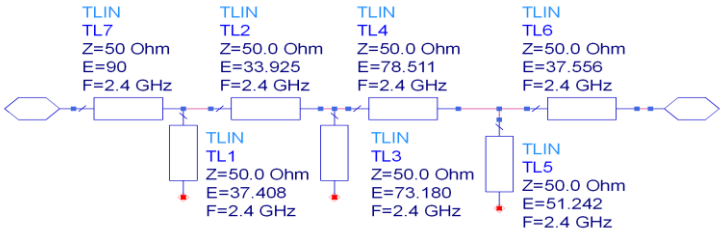

Figure 7. Input Matching Network realized using Microstrip Lines

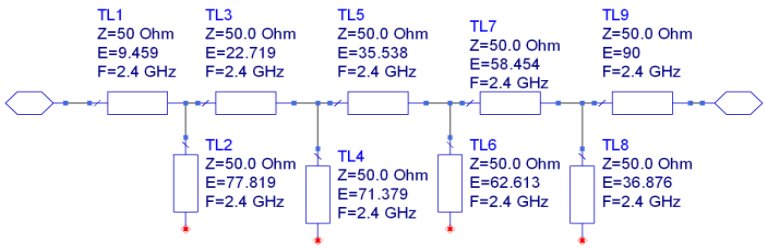

Figure 8. Output Matching Network realized using Microstrip Lines

3.5 Schematic Simulation

The complete schematic design of the power amplifier is shown in Figure 9. S parameter simulation and Harmonic balance simulation are carried out to measure the performance of schematic designed power amplifier. Figure 10 shows the harmonic balance simulation result of schematic power amplifier. The power amplifier gives an output power of 35.610 dBm for the input power of 21.253 dBm with a gain of 14.2 dB. The S Parameter simulation result shows (Figure 11) at 2.4 GHz amplifier achieves return loss (S_{11}) of 20.225dB and gain (S_{21}) of 16.558 dB. The Bandwidth is obtained by measuring the range of frequencies in which gain is 3 dB down the maximum gain value. The Bandwidth value of the power amplifier is 54MHz in the 2.4 GHz ISM Band.

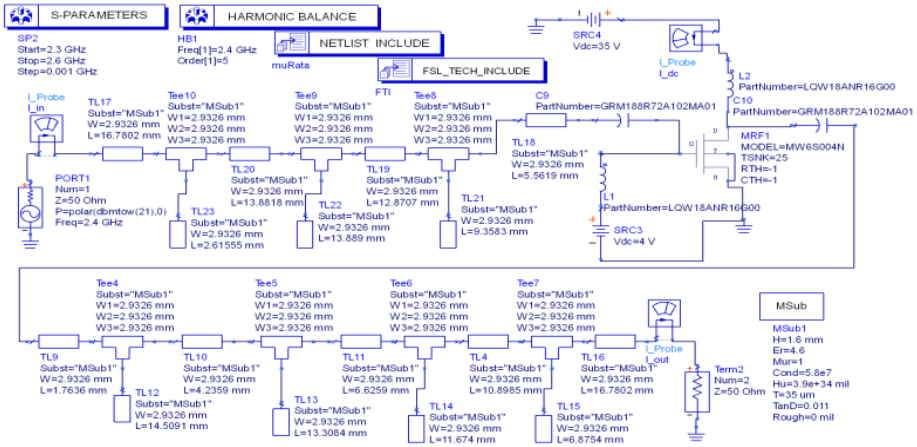

Figure 9. Schematic design of Power Amplifier

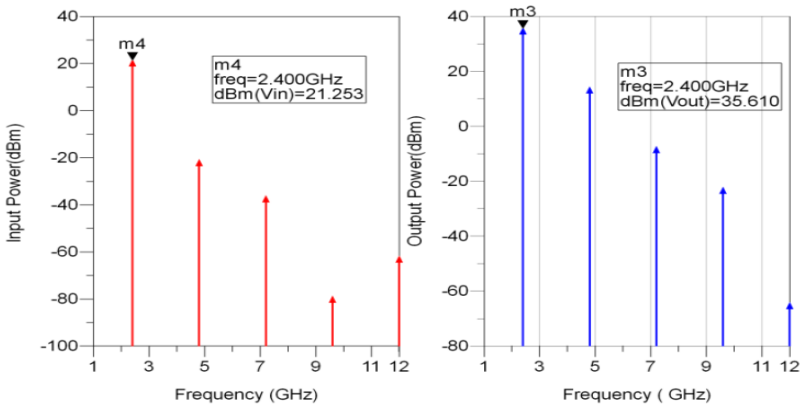

Figure 10. Harmonic balance simulation of Schematic design

3.6 Hardware Software Co- Simulation

The ADS schematic of Class A power amplifier setup with matching networks is realised in the form of microstrip lines. The microstrip transmission lines are converted into layout, later this layout design is fabricated on printed circuit board (PCB). In the PCB the discrete components needed for power amplifier such as capacitor, inductor and Si-LDMOS transistor are soldered to realize it as hardware. Another approach is to verify the hardware performance in Co-simulation. Here the layout design and discrete components are integrated for verifying the circuit behaviour [13].

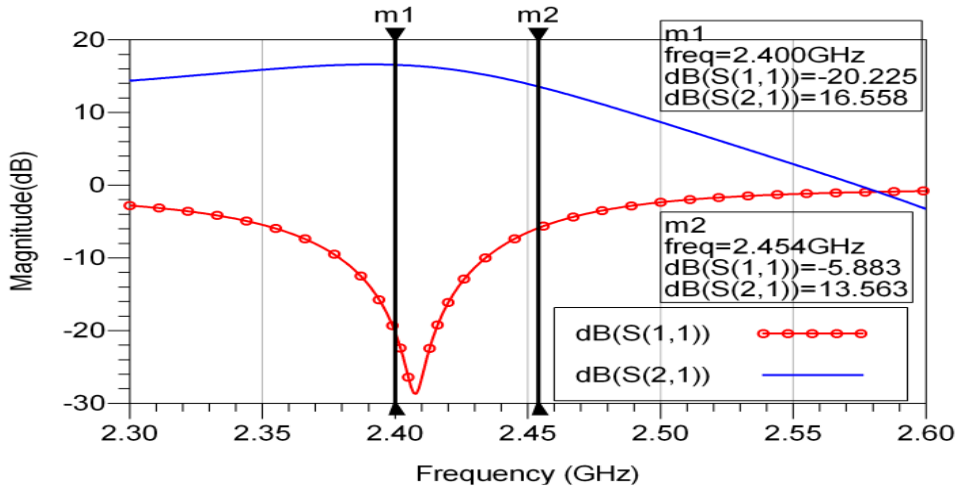

Figure 11. S- Parameter simulation of Schematic design

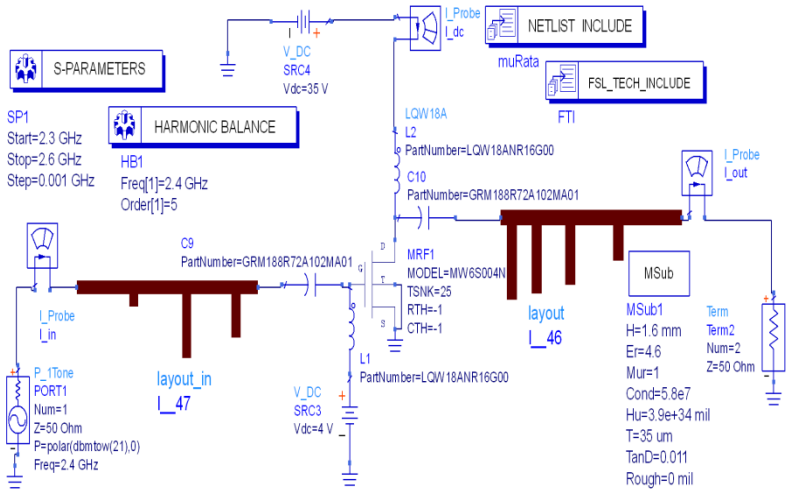

Figure 12. Co-simulation analysis of the power amplifier

The circuit can be generated into a layout by selecting Layout →Generate /Update Layout. ADS will convert the microstrip nature of schematic design into a layout. When it is done, a layout window pops up, showing the layout. This layout generation is separately done for input matching and output matching. The layout generated for the power amplifier circuit is brought to the new schematic and the transistor along with lumped components are connected and simulated. The lumped inductor and capacitor component models are obtained from the component manufacturer (murata). This type of simulation technique is called as Co-simulation [14]. The Co-simulation gives the result which will be same as the result obtained after fabrication of the hardware.

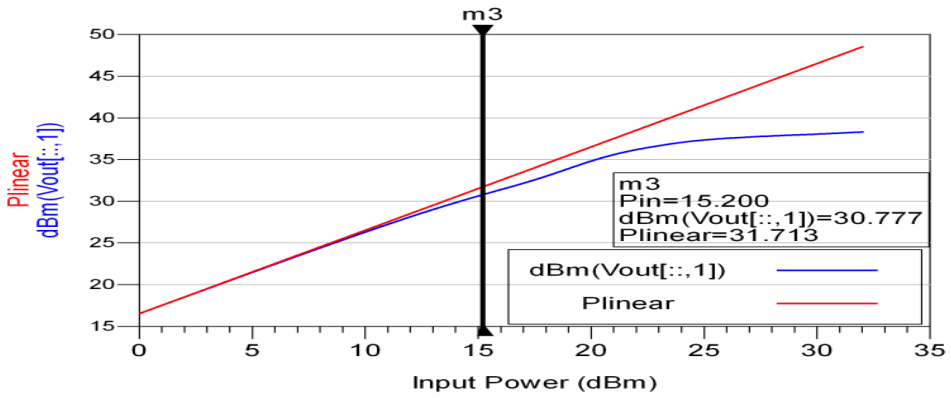

Figure 13. Illustration of 1-dB compression point

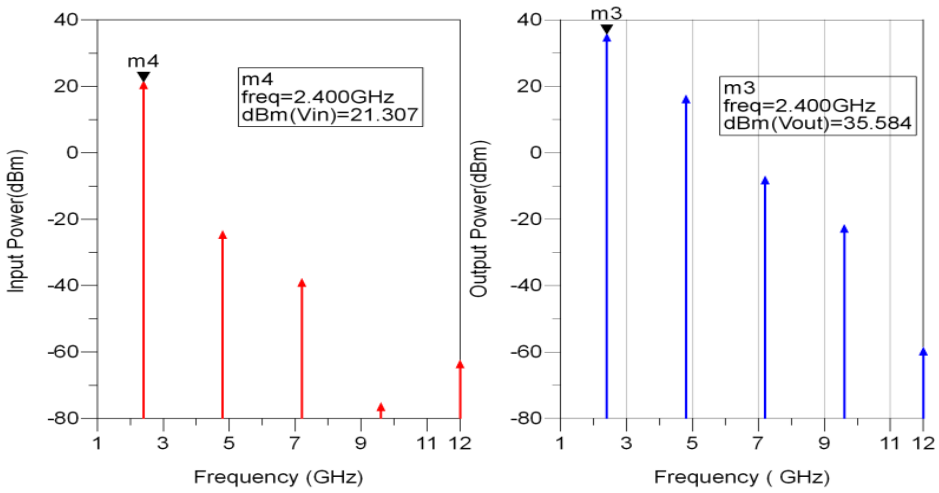

Figure 14. Harmonic balance result of Co-simulation design

Figure 12. shows the power amplifier circuit used for co-simulation analysis. The microstrip based matching sections are made up of low cost FR4 substrate with dielectric constant 4.6 and substrate thickness of 1.6 mm. The linear behaviour of power amplifier is indicated in 1-dB compression point graph as shown in Figure 13. The 1-dB compression point is at 15dBm of input power. The harmonic balance result of Co-simulation is illustrated in Figure 14. It shows there is not much deviation between schematic design result and Co-simulation result. This justifies the hardware realization of the proposed LDMOS power amplifier will ensure the gain value of more than 15 dB at the ouput power levels of 30 dBm.

IV. CONCLUSION

In this work, a silicon LDMOS based ISM band RF power amplifier is designed. Power amplifier design using Si-LDMOS is a cost effective approach. Class A power amplifier is chosen for our design because of more linearity. The power amplifier is built on Epoxy-FR4 board. The Schematic and layout Co- simulation is performed using Agilent ADS 2011. The result shows a gain of 16.558 dB, power added efficiency of 61.897 and the output power of 35.61 dBm at 2.4 GHz. The layout of the amplifier is generated and co-simulation is performed to verify the schematic results. All the parameters of the amplifier meet the design specifications, revealing the correctness and feasibility of the design method. The simulated result shows the usage of the proposed LDMOS based power amplifier for wireless base station requirements.

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