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LOW POWER ARCHITECTURE FOR ASIP'S: BASED ON ADIABATIC SWITCHING PRINCIPLES

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ABSTRACT

Power minimization is one of the primary concerns in today VLSI design methodologies because of two main reasons one is the long battery operating life requirement of mobile and portable devices and furthermore, the number of gates per chip area is constantly increasing, while the gate switching energy does not decrease at the same rate, so the power dissipation rises and heat removal becomes more difficult and expensive. In this paper a low power architecture for ASIP is proposed. Proposed architecture is designed using adiabatic switching principles. Proposed adiabatic ASIP is tested using VHDL. The results show that performance of adiabatic ASIP is better than other contemporary ASIPs

KEYWORDS: *Adiabatic, Reversible Logic, ASIP, ASIC, Instruction set*

I. INTRODUCTION

Power minimization is one of the primary concerns in today VLSI design methodologies because of two main reasons one is the long battery operating life requirement of mobile and portable devices and furthermore, the number of gates per chip area is constantly increasing, while the gate switching energy does not decrease at the same rate, so the power dissipation rises and heat removal becomes more difficult and expensive. Then, to limit the power dissipation, alternative solutions at each level of abstraction are proposed.

1. At the Device (Technology) level, techniques such as VT reduction, multi-threshold voltages, gate oxide thickness, and length and width variations are more common.
2. At Circuit level, techniques such as use of alternate devices, network re-structuring, at Logic level, techniques such as use of alternate logic styles, energy recovery methods are common.
3. At Architecture (System) level and Algorithmic level, techniques such as use of parallel structures, pipelining, state machine encoding, alternate encoding methods, etc. are more common. One such method at circuit and logic level, the energy recovery method, which employs reversible logic concepts.

In present work attempts are made to design an adiabatic ASIP. The present work focuses on limiting the power dissipation at architecture (System) level and instruction set level, techniques such as use of parallel structures, state machine encoding, alternate encoding etc. are used. Rest of the paper is organized as follows the section to covers literature review whereas section3 gives Structure of Proposed adiabatic ASIP in section 4 Design of the adiabatic ASIP is covered finally section 5 covers results and discussions at the end paper is completed with conclusion and future research directions.

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II. LITERATURE REVIEW

In 2003, Youngjoon Shin, Hanseung Lee, Yong Moon, and Chanho Lee in their work proposed a 16-bit adiabatic low-power Microprocessor core. The processor consists of control block, multi-port register file and ALU. A simplified four-phase clock generator is designed to provide supply clocks for adiabatic processor. All the clock line charge on the capacitive interconnections is recovered to recycle the energy. Adiabatic circuits are designed based on ECRL (efficient charge recovery logic) and 0.35 ㎛ CMOS technology is used. Simulation results show that the power consumption of the adiabatic Microprocessor core is reduced by a factor of 2.9~3.1 compared to that of conventional CMOS Microprocessor. Later in 2004, Youngjoon Shin, Chanho Lee, and Yong Moon presented a low power 16-bit adiabatic reduced instruction set computer (RISC) microprocessor with efficient charge recovery logic (ECRL) registers. The processor consists of registers, a control block, a register file, a program counter, and an arithmetic and logical unit (ALU). Adiabatic circuits based on ECRL are designed using a 0.35 μm CMOS technology. An adiabatic latch based on ECRL is proposed for signal interfaces for the first time, and an efficient four-phase supply clock generator is designed to provide power for the adiabatic processor. A static CMOS processor with the same architecture is designed to compare the energy consumption of adiabatic and non-adiabatic microprocessors. Simulation results show that the power consumption of the adiabatic microprocessor is about 1/3 compared to that of the static CMOS microprocessor. Ravish Aradhya H V, Praveen Kumar B V, Muralidhara K N in (2011) proposed in their novel work proposed a design of full Adders using synthesizable, low quantum cost, low garbage output Peres gates. In their work data transfer, addition, subtraction, increment, decrement and many other Arithmetic operations are realized using reversible gates. Technology advances in VLSI designs offer exponentially shrinking device dimensions and exponentially growing circuit complexities. However, device scaling is critically limited by the power dissipation; demanding for better power optimizations methods. Reversible Logic is becoming more and more prominent special optimization technique having its applications in Low Power CMOS designs, Quantum Computing and Nanotechnology. ALU is a fundamental building block of a central processing unit (CPU) in any computing system; reversible arithmetic unit has a high power optimization on the offer. By using suitable control logic to one of the input variables of parallel adder, various arithmetic operations can be realized. In this paper, as a part of ALU design, a Reversible low power control unit for arithmetic operations is proposed. Akanksha Dixit, Vinod Kapse in their work stated that reversible logic has received great attention in the recent years due to its ability to reduce the power dissipation which is the main requirement in low power digital design. It has wide applications in advanced computing, low power CMOS design, Optical information processing, DNA computing, bio information, quantum computation and nanotechnology. Conventional digital circuits dissipate a significant amount of energy because bits of information are erased during the logic operations. Thus, if logic gates are designed such that the information bits are not destroyed, the power consumption can be reduced dramatically. The information bits are not lost in case of a reversible computation. This has led to the development of reversible gates. ALU is a fundamental building block of a central processing unit (CPU) in any computing system; reversible arithmetic unit has a high power optimization on the offer. By using suitable control logic to one of the input variables of parallel adder, various arithmetic operations can be realized. In this paper, ALU based on a Reversible low power control unit for arithmetic & logic operations is proposed. In our design, the full Adders are realized using synthesizable, low quantum cost, low garbage output DPeres gates. This paper presents a novel design of Arithmetic & Logical Unit using Reversible control unit. These Reversible ALU has been modeled and verified using Verilog and Quartus II 5.0 simulator. Comparative results are presented in terms of number of gates, number of garbage outputs, number of constant inputs and Quantum cost. Shipra Upadhyay, R. K. Nagaria and R. A. Mishra in their paper, presented the design and experimental evaluation of complementary energy path adiabatic logic (CEPAL) based 1 bit full adder circuit. A simulative investigation on the proposed full adder has been done using VIRTUOSO SPECTRE simulator of cadence in 0.18μm UMC technology and its performance has been compared with the conventional CMOS full adder circuit. The CEPAL based full adder circuit exhibits the energy saving of 70% to the conventional CMOS full adder circuit, at 100 MHz frequency and 1.8V operating voltage. Ismo Hänninen, Hao Lu, Enrique P. Blair, Craig S. Lent, and Gregory L. Snider in 2014 stated that emerging devices promise energy-efficient computing on a massively parallel scale, but due to the extremely high integration density the previously

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insignificant dissipation due to information erasure (destruction) becomes a prominent circuit design factor. The amount of heat generated by erasure depends on the degree of logical reversibility of the circuits and successful adiabatic charging. In this paper, we design an adiabatic arithmetic-logic unit to prototype the locally-connected Bennett-clocked circuit design approach. The results indicate one or two orders-of-magnitude energy savings in this physical circuit implementations vs. standard static CMOS. Previous work on computer arithmetic suggests that common hardware implementations erase much more information than would be required by a theoretical minimal mapping of the addition operation. A Bennett-clocked approach can reach the theoretical minimum number of bit erasures in the binary addition, though simulations show that a transistor technology has energy loss due to parasitic components that can exceed the information loss heat. In this paper, we describe the relationship between adiabatic and logically reversible circuits, and predict the potential of the arithmetic implementations based on quantum-dot cellular automata, which enable the full benefits of reversible, locally connected circuits to be realized. Sriraj Dheeraj Turaga, Kundan Vanama, Rithwik Reddy Gunnuthula and K.Jaya Datta Sai (2014) implemented a 4-bit Arithmetic Logic Unit (ALU) using Complementary Energy Path Adiabatic Logic (CEPAL). This static adiabatic logic has proved its advantage through the minimization of the 1/2CVdd2 energy dissipation occurring every cycle. Firstly, the performance characteristics of CEPAL 4-to-1 multiplexer and full adder are compared against the conventional static CMOS logic counterpart to identify its adiabatic power advantage. Finally, A 4-bit Arithmetic Logic Unit (ALU) is implemented with both the technologies and comparisons have been made. The analysis is carried out using the industry standard EDA design environment using 250 nm technology libraries from Tanner. The results prove that the CEPAL 4-bit ALU is 55% more power efficient than the CMOS 4-bit ALU at 100MHz and at 2.5V operating voltage.

Sunil Jadhav, Sachin Borse in 2015 presented that there are so many strategies implemented to reduce the power consumption in CMOS digital design. Many of them are based on complement form and clock signals. In CMOS digital design power consumption can be reduced by reducing the supply voltage, decreasing capacitance and reducing the switching activities. These techniques are not suitable in today's CMOS design scenario. So many researchers are working on new design techniques which will help in reducing the dynamic power consumption. Most of the research is focused on adiabatic logic which is proved to be the excellent technique to design the low power digital circuits. In this paper they focused on the adiabatic logic with complementary energy path dual pass transistor logic (DPL-CEPAL). Conventional NAND, NOR and EX-OR/NOR gates are compared with the DPL-CEPAL NAND, NOR and EX-OR/NOR gates. It was suggested that DPL-CEPAL technique is superior to conventional technology as far as power consumption is concerned. This DPL-CEPAL technology can be used to design the full adder cell and multiplier cell which are the core part of any ALU processor.

A literature review was carefully carried out and the shortcoming and gaps in efficient design of Adiabatic ASIP were analyzed. It is evident from the review that at present Adiabatic logic based ASIPs does not exist. Therefore present work has lot of research potential.

III. STRUCTURE OF PROPOSED ADIABATIC ASIP

In present work the aim is to design low power architecture for Application Specific Integrated Processor (ASIP's) based on adiabatic switching principles. An application-specific instruction set processor (ASIP) is a component used in system-on-a-chip design.

General purpose processors are designed to execute multiple applications and perform multiple tasks. It can be quite expensive especially for small devices that are designed to perform special tasks. Also general purpose processors might lack high performance that a certain task required. Therefore, application specific processors emerged as a solution for high performance and cost effective processors. Application specific processors have become a part of our life's and can be found almost in every device we use on a daily basis. Devices such as TVs, cell phones, and GPSs they all have a form of application specific processors. An application specific processor combines high performance, low cost, and low power consumption. The instruction set of an ASIP is tailored to benefit a specific application. This specialization of the core provides a tradeoff between the flexibility of a general purpose CPU and the performance of an ASIC.

The design optimization may be done on components of the data path like ALU, registers etc. The basic component of the arithmetic section of the ALU is a parallel adder. A parallel adder is constructed with

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a number of full adders and as here we have to design a 8 bit ALU, we are using eight full adders. By controlling the data inputs to the parallel adder, it is possible to get different type of micro operations. In arithmetic operations there are add, minus, while in logical operations there are NOT, OR, AND, and so on. The above operations can be realized by using reversible logic gates, based on the principal of adiabatic switching, through which we can reduce the energy consumption. The proposed ASIP consist of following important blocks:

- Arithmetic logic unit (ALU),
- Shifter unit (SHU),
- Accumulator (AC),
- Instruction Pointer (IP),
- Status Register (SR),
- Memory Address Register (MAR),
- Instruction Register (IR) and
- Control Unit (CTRL).

IV. DESIGN OF ADIABATIC ASIP

The adiabatic ASIP design includes, designing of all the blocks of Adiabatic ASIP discussed in section 3 such as registers, a control unit, a program counter (PC), a register file, a shifter, and an ALU etc. to be designed using hierarchical structural modelling. That is all the blocks will be designed using basic PFAL gates. The block diagram of the proposed adiabatic ASIP is shown in Fig. 1.

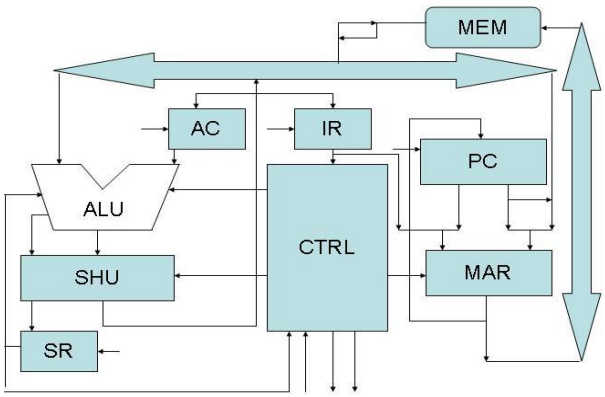

Figure 1: Block diagram of Adiabatic ASIP

All the blocks of the proposed adiabatic ASIP are designer using basic PFAL Gates. The control block receives instruction codes from a PFAL register and generates suitable control signals with the matching operation phases. The PC value is determined by an auto incrementer or by a value in the register file. The ALU is an 8-bit arithmetic and logical unit. Figure 6 shows the block diagram of the ALU.

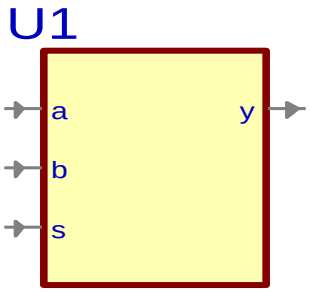

Figure 2: Block Diagram of Adiabatic ALU

The 8-bit ALU is the most important component of the adiabatic ASIP. All the instructions whether logical or arithmetic are processed by the ALU. The signal Description of the ALU

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is given in table 1. 'A' and 'B' are the input buses. 'S' denotes the select line which instructs ALU to perform Operation and 'Y' is the output bus.

Table 1: Signal Description of Adiabatic ALU

S.NO	SIGNAL NAME	SIGNAL TYPE	DESCRIPTION
1.	A	INPUT	BUS
2.	B	INPUT	BUS
3.	S	INPUT	SELECT LINE
4.	Y	OUTPUT	BUS

V. RESULTS AND DISCUSSIONS

Adiabatic ASIP is implemented using VHDL and Simulated using ACTIVE HDL 8.1 Simulator. The individual gate functionality and the overall logic is implemented using Structural style of Modeling and this paper shows Logical diagram of an adiabatic ASIP shown in fig.3.

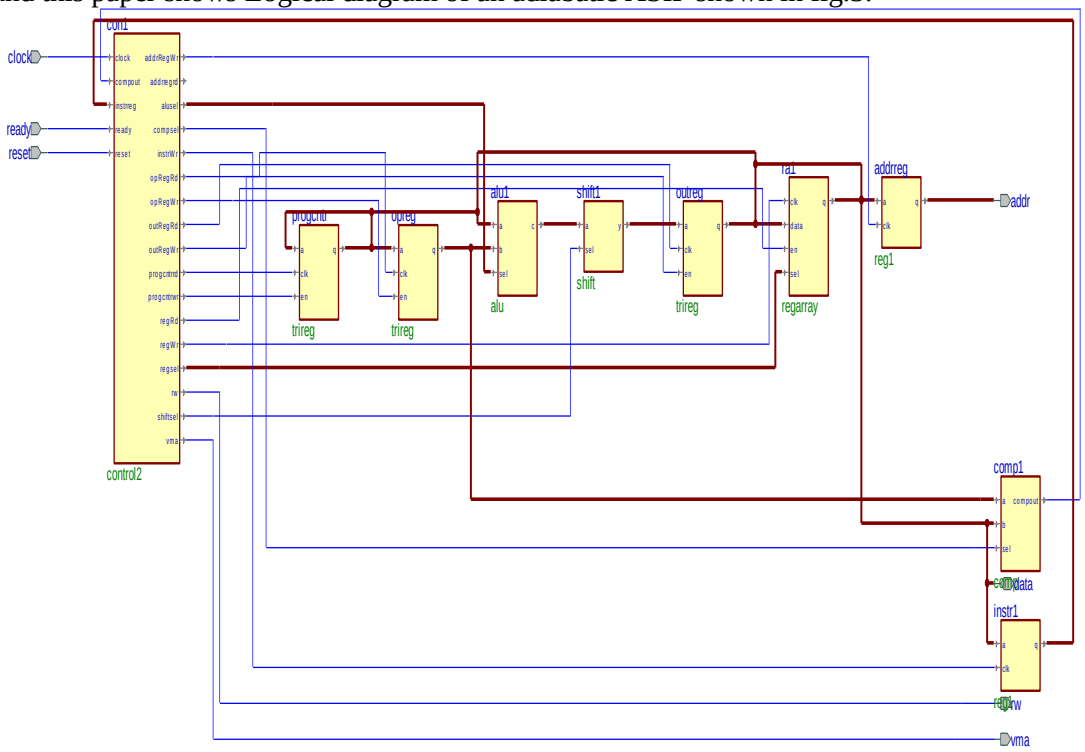

Figure 3: Logical diagram of an adiabatic ASIP

The energy consumption per operation and the adiabatic gain of the PFAL arithmetic units working at 10, 20, 30 MHz are reported in Table 5.2. The consumption of the equivalent CMOS ASIC and ASIP are also reported for comparison. Since we are dealing with a semi-custom design built of fixed cells, the circuits are not optimized for the particular point of operation, such as modifying transistor dimensions or scaling the supply voltage. The results show that semicustom adiabatic ASIP unit is more energy efficient over the entire frequency range. The Power Comparison of Adiabatic ASIP with CMOS ASIC and CMOS ASIP is shown in fig. 4.

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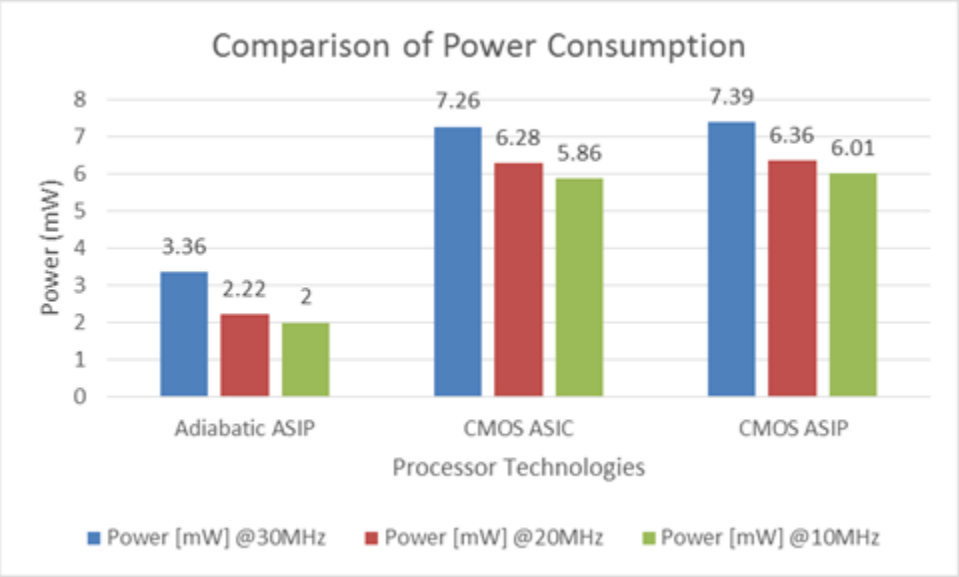

Figure 4: Power Comparison of Adiabatic ASIP with CMOS ASIC and CMOS ASIP

VI. CONCLUSION

In this paper, adiabatic ASIP has been proposed. An 8-bit adiabatic ASIP is designed using a using PFAL technology. It includes PFAL gates, which make up the PFAL registers which acts as storage element. A conventional static CMOS microprocessor with the same structure is used to compare the power consumption with different clock frequencies. For energy and functional simulation extracted gate level net-lists from the VHDL was used to verify that the adiabatic ASIP works correctly. The energy consumption of the adiabatic ASIP is significantly improved compared to that of the conventional static CMOS ASIP. The prototype design of an 8-bit adiabatic ASIP with PFAL based circuits shows the feasibility of adiabatic circuits in low power applications. adiabatic ASIP has great improvement over existing designs.

VII. FUTURE WORK

Adiabatic ASIP is developed by applying a set of analysis and design techniques to create systems with improved dependability. As new technologies are developed and new applications arise, new low power design approaches are also needed. Some additions to enable performance improvements as a part of future work are suggested such as a timing constraints can be provided during simulation. some of the developments that can be done for in design of adiabatic ASIP to improve its performance or increase its functions such as Pipelining the ALU, include more number of input bits for the ALU, adding more IO Operations etc.

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