AN EFFICIENT ADIABATIC SWITCHING CIRCUIT DESIGN FOR LOW POWER APPLICATIONS

Amit Saxena[1], Kshitij Shinghal[2], Deepti Shinghal[1]

[1]Assistant Professor, [2]Associate Professor,
Deptt. of E& C Engg, Moradabad Institute of Technology, Moradabad, India
[1]Research Scholar, Monad University, Hapur, India

ABSTRACT

Ever-increasing demand of computational capacity and power constraints of hand held and battery operated portable devices has lead to the requirement of Low power memories. The power consumption of SRAM varies widely depending on how frequently it is accessed; it can be as power-hungry as dynamic RAM, when used at high frequencies, and some ICs can consume many watts at full bandwidth. On the other hand, static RAM used at a somewhat slower pace, such as in applications with moderately clocked microprocessors, draws very little power and can have a nearly negligible power consumption when sitting idle – in the region of a few micro-watts. Several techniques have been proposed to manage power consumption of SRAM-based memory structures. In this paper a robust adiabatic SRAM is designed. The main aim is to use adiabatic switching circuits to compensate throughput degradation, so a medium throughput for SRAM can be achieved. Proposed architecture is designed using adiabatic switching principles. Proposed adiabatic SRAM is tested using OrCAD Pspice. The results show that performance of adiabatic SRAM is better than other contemporary SRAMs

KEYWORDS: *Adiabatic, Reversible Logic, Memories, SRAM*

I.   INTRODUCTION

Designing electronic systems using digital techniques has become a well-accepted standard with electronic design community. The precision and speed of any computational block in digital design can be increased by just widening the data bus and making computational blocks compatible with widened data bus. Thus a complex digital electronic system handles wide data buses, addresses large memory space and embeds the logical and computational blocks with appropriate data bits to match the widened data bus. Due to the typical features of CMOS technology, for integrating complex systems in small silicon area with fairly low power dissipation at speeds demanded by most of the applications, CMOS VLSI has been the obvious choice of designers. About 90% of the total electronic systems use CMOS technology at the back end.

CMOS technology has as edge over other device technologies as far as power dissipation is concerned. The three contributory factors to the total power dissipation in CMOS are : a) Static Power Dissipation under steady state due to reverse leakage current of p-n junctions and subthreshold leakage current ($\approx$ 15% contribution to total power dissipation) , b) Dynamic Power Dissipation due to charging and discharging of load capacitance during switching ($\approx$ 70-75% contribution to total power dissipation) and c) Short Circuit Power Dissipation due to direct low resistance path between supply and ground again during switching. ($\approx$ 10% contribution to total power dissipation). Hence number of solutions at architectural level and circuit level have been proposed in the literature to primarily reduce dynamic power dissipation and then leakage & short circuit power dissipation of CMOS circuits. Though, over a period of time an appreciable reduction in power dissipation and hence energy consumption has been

achieved, one of the draw- backs of CMOS circuits is that energy is continuously drained out from the power supply. Adiabatic logic technology has been proposed as one of the ways to con- serve and recover energy thereby offering energy efficient solutions to electronic systems.

In present work attempts are made to design an adiabatic SRAM. The present work focuses on limiting the power dissipation at System level. Rest of the paper is organized as follows the section to covers literature review whereas section 3 gives Structure of Proposed adiabatic SRAM in section 4 Design of the adiabatic SRAM is covered finally section 5 covers results and discussions at the end paper is completed with conclusion and future research directions.

II.　LITERATURE REVIEW

Yibin Ye, Dinesh Somasekhar, and Kaushik Roy in 1996 described in their paper titled "On The Design of Adiabatic SRAMs" that the design of low-power circuits, adiabatic logic shows great promise. However, research till date have concentrated on adiabatic logic circuits/families. Today's VLSl systems integrate random logic, mega modules and memories. Hence, the success of adiabatic circuits will depend on the efficient implementation of not only random logic, but also the other components of a VLSI system. They presented a design of adiabatic Static RAM, which can be implemented without greatly increasing area or circuit complexity. The design addresses the issue of building ultra-low power memory circuits in a VLSI system. Our results for a 4Kb block of memory core indicates energy savings of approximately 75% for both read and write operations. Higher power savings are achieved in the address decoder and I/O drivers [13]. In 2004 Jianping Hu, Xu Tiefeng, Junjun Yu, Yinshui Xia in their novel work presented a dual transmission gate adiabatic logic (DTGAL) suitable for driving large capacitance was presented. DTGAL, has no non-adiabatic energy loss on output loads by using feedback control from next-stage buffer outputs. The minimization of energy consumption was investigated by choosing the optimal size of DTGAL circuits. A 64×64-b adiabatic SRAM was designed. The proposed DTGAL circuits was used to recover the charge of large switching capacitance on bit-lines, word-lines, and address decoders in fully adiabatic manner. The power consumption of the proposed SRAM was significantly reduced as the energy transferred to large capacitance buses was mostly recovered. Energy and functional simulations were performed using the net-list extracted from the layout. There HSPICE simulation results indicated that their SRAM attains energy savings of 65% to 90% as compared with the conventional CMOS implementation for clock rates ranging from 25 to 200 MHz [14]. In 2006 Jun-Jun Yu, Peng-Jun Wang in their work described about adiabatic logic circuits and analyzed its power dissipation. They proposed a new adiabatic logic circuit adopting two-phase power clocks - clocked transmission gate adiabatic logic (CTGAL) circuit was presented. CTGAL circuit was used to design a novel adiabatic SRAM, and its bootstrapped NMOS transistors and CMOS-latch structure could recover the charge of large switching capacitances on word-lines, write bit-lines, sense amplified lines and address decoders in a fully adiabatic manner. Using the parameters of TSMC 0.25mum CMOS device, the adiabatic SRAM based on CTGAL circuit was simulated by HSPICE. The simulation results indicated that this SRAM had correct logic function and the character of clearly low power circuits [15]. Later in 2012 Sunil Jadhav, Vikrant, Munish Vashisath stated that Power consumption has become a critical concern in both high performance and portable applications. They further quoted that methods for power reduction based on the application of adiabatic techniques to CMOS circuits have recently come under renewed investigation. In thermodynamics, an adiabatic energy transfer through a dissipative medium is one in which losses are made arbitrarily small by causing the transfer to occur sufficiently slowly. In their work adiabatic technique were used for reduction of average power dissipation. Simulation of 6T SRAM cell has been done for 180nm CMOS technology. It showed that average power dissipation was reduced up to 75% using adiabatic technique and also depicted the effect on static noise margin [16]. Ankita Singh, Vishal Moyal in 2014 analysed and stated that different adiabatic approach for the 8t SRAM cell in her work. They designed an 8T SRAM cell to perform the write and read operations which employs a single bit line scheme. An SRAM is considering in the most development stage today, with its different variations as well as to support low power application. Stability factor and Leakage power is becoming the most important factor on SRAM (Static Random Access Memory) cells. A novel 8T SRAM cell design was considered reducing the leakage and also reducing the stability issues as compare to 6T SRAM cell. Now by including adiabatic circuit into 8T SRAM cell has become a new promising approach on consumption of power.

The different adiabatic SRAM circuits proposed in the resent years are outlined in her research [17]. Poonam Boora, Ramnish Kumar carried out simulation of 6T SRAM using 180nm CMOS technology and TANNER TOOLS. In the current VLSI digital circuits, power consumption is one of the main design concerns. Power consumption has become a critical concern in both high performance and portable applications. In their work two low power techniques are being discussed. One is adiabatic technique and other is Bulk-biased technique. The performance of conventional 6T SRAM circuit is compared with adiabatic 6T SRAM circuit and bulk-biased 6T SRAM circuit. Using these techniques a greater degree of power reduction has been achieved [18].

R. Sindhu, Shivani Patel and P.Ram Mohan Rao in 2015 stated SRAM is a major source to store the data for a long time. The major reason for the power leakage in SRAM could be a bitline. This leakage should be reduced for better performance of the circuit and it can avoid the Chip damage. The manufacturing by using this circuit contains poor performance and high leakage. In their work power is reduced, by designing the circuit using single bitline. In single bitline SRAM only one bitline is used for read operation and the voltage level at another bitline node is remains low. So it has high Static Noise Margin compared to the two bitline SRAM. To reduce the extra leakage from this circuit while recycling the Negative Bias Temperature Instability based SRAM circuit is implemented. This reduces the leakage from the SRAM circuit and also increases the read stability in the circuit [19]. In 2015 Sriramoju Nagarani discussed about rapid advances in the field of very large scale system designs brought memory circuits are continuously regulated and in turn, more number of cells could made possible to integrate on small chip. However in Nano scale SRAM there is large variation of threshold voltage occurs. To slove Vt variation problem in SRAM in their work we proposed the adiabatic SRAM cell and later we introduce a NBTI SRAM which effectively reduces the problem was given [20]. Nikita V. Keche and Ashish E. Bhande in their survey conducted in 2015 said that to minimize energy consumption, low voltage circuits are needed. Static random access memory (SRAM) is a key element in wide variety of applications and so considering the need of SRAM cell, NVSRAM have been proposed. NVSRAM provide fast power on off speeds and information doesn't loss even if the power supply is turned off. This paper provide new approach towards designing and modeling of NVSRAM cell using volatile SRAM core. The nonvolatile characteristic and the nanoscale geometry of NVSRAM increases the packing density with CMOS processing technology provides new approaches towards power management, without loss of stored information, Hence has potential for major saving in power dissipation. Also NVSRAM cell has scope for speed improvement as the technology matures [21]. Weiqiang Zhang et. al. in their work tried to reduce the increasing power dissipation of the SRAM. The proposed SRAM was realized by PAL-2N (pass-transistor adiabatic logic with NMOS pull-down configuration) to reduce its dynamic energy consumption. The GLB (gate-length biasing) and DTCMOS (dual-threshold CMOS) techniques are used to reduce its leakage consumption. An improved storage cell was used to reduce the power dissipation of the storage array. The proposed SRAM was based on PAL-2N with GLB and DTCMOS techniques is investigated with different source voltages in terms of energy dissipation and maximum operating frequency. All circuits were simulated with HSPICE using SMIC 130nm CMOS technology. The results suggested that the proposed SRAM attain 80% energy saves compared with the static SARM at 1.2V source voltage. In addition, the simulation results also suggested that the super-threshold adiabatic SRAM operating in medium strong inversion regions achieves low energy dissipation with reasonable operating speed [22]. Santhiya.V and Mathan. N in 2015 showed that the power consumption is a major concern these days for long operational life. Although various types of techniques to reduce the power dissipation has been developed. One of the most adopted method is to lower the supply voltage. Techniques based on replica circuits which minimize the effect of operating conditions variability on the speed and power. In their work different static random access memory are designed in order to satisfy low power, high performance circuit and the extensive survey on features of various static random access memory (SRAM) designs were reported [23]. Priyanka Ojha, Charu Rana in 2015 showed that various adiabatic logic circuits can be used for minimizing the power dissipation. To enhance the functionality and performance of circuit two adiabatic logic families PFAL and ECRL have been used and compared with CMOS logic circuit design. In their work, A MASTER-SLAVE D flip-flop was designed by the use of SPICE simulation on 90nm technology files. The simulation result showed that PFAL is a better energy saving techniques then ECRL logic circuit [24]. Saravanan.S et.al. in 2015 Solved various power related issues of CMOS, FinFET is one of the promising and better technologies without sacrificing reliability and performance

for its applications and the circuit design. To minimize short channel effects, FinFET is used. In proposed work SRAM was designed using a CMOS technology and that technique gives a 98% advantage of reducing a leakage power. The power consumption and delay is less for Stack and SVL technique [25].

From the above literature review it can be clearly observed that there exists a huge gap between the predicted power consumption of Memories (SRAMs) and real practical power consumption of SRAMs and there is a lot of scope of improving power consumption of SRAMs. The adiabatic SRAM seems to be a promising solution for fulfilling efficient utilization of power in SRAMs.

III.   STRUCTURE OF PROPOSED ADIABATIC SRAM

The proposed adiabatic SRAM cell design is shown in Figure 1. The proposed design focuses on making the basic inverter pair of the memory cell effective for low voltage operations. The 4 transistors forms one inverter pair and other 4 forms another adiabatic inverter pair. The transistors pairs are also used as access transistors for the bit line. At low voltages, the cross-coupled inverter pair stability is of major concern during the transition and read operation, to improve the stability of data read (0 and 1), Schmitt trigger configuration is used. In this design, Schmitt trigger increases or decreases the switching threshold of an inverter depending on the direction of the output transition. This adaptation is achieved with the help of series transistor feedback technique with reduced transistor count for the Schmitt trigger operation.
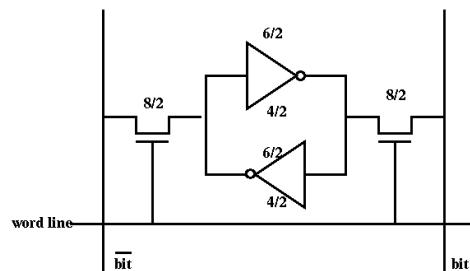

Figure 1: Proposed adiabatic SRAM cell design

IV.   DESIGN OF THE ADIABATIC SRAM

The adiabatic SRAM design is based on Dynamic Voltage Scaling (DVS) technique to reduce the leakage current and static power of the adiabatic SRAM cells and also retains the data stored during the idle mode. The leakage current reduces with operating voltage scaling in deep submicron processes because of short channel effects. The basic idea of the adiabatic SRAM is the use of two pass-transistors N4, N5 that provide different ground supply voltages to the adiabatic SRAM cell for normal and idle modes. The pass transistor N4 provide a positive voltage when the adiabatic SRAM cell is in idle mode and another pass transistor N5 provide a virtual ground when the cell is in active mode. The operating voltages of a memory cell are varied to switch between the active and idle (standby) modes that will give the less Leakage power significantly. The key idea of the adiabatic SRAM is the use of two pass-transistors that provide different ground supply voltages to the memory cell for normal and sleep modes. These pass- transistors provide a positive ground supply voltage when the cell is inactive and connect the cross-coupled inverters to the ground supply during normal operation to function as a conventional 6T-cell. The operating voltages of an array of memory cells are varied to switch between the active and stand-by modes and thus reducing the leakage power significantly. Both the access transistors (M5, M6) are high-Vt devices to further reduce the bit line leakage. Each of the pass gate used to control the source voltages of the NMOS transistors in the cross-coupled inverter is also a high-V, device to control the leakage current through these two pass transistors from the positive control voltage v to ground). None of the nodes is left floating when the cell is not in use and this ensures the stability of the stored data with no additional complexity or circuitry. Since the capacitance of the ground supply lines is significantly less than that of the wells, this approach has improved transition time and energy as compared to others. Moreover, since the source voltage, as opposed to substrate voltage, is used to

control the V, of the NMOS transistors during the sleep mode, the inherent problems associated with body bias are totally eliminated.

Reduction of the gate leakage current in the adiabatic SRAM cell can be done. The idea behind the adiabatic SRAM is to provide different ground levels of the memory cell in active and idle modes. During idle mode the positive voltage more than ground reduces the gate leakage and sub threshold currents of the adiabatic SRAM cell.
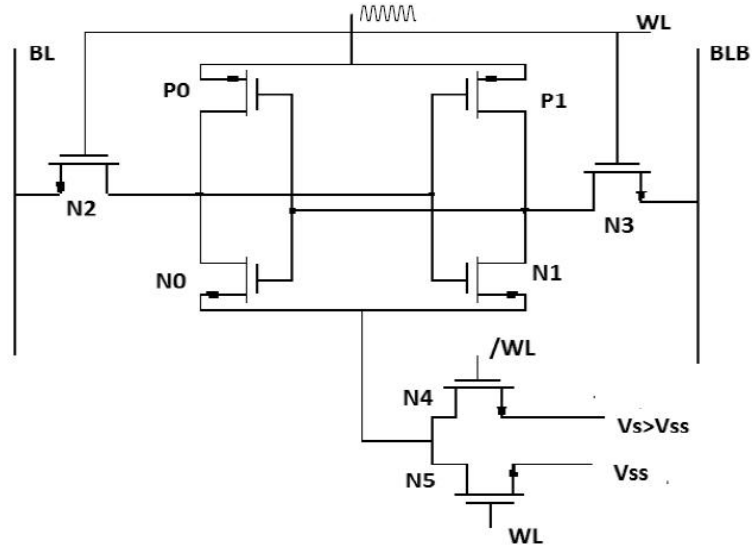

Figure 2: Basic Adiabatic SRAM cell

V.   RESULTS AND DISCUSSIONS

Adiabatic SRAM is implemented using OrCad Pspice Simulator. The individual gate functionality and the overall logic is implemented using Structural style of Modeling .

It is an asynchronous SRAM with capacity of 2K×8 bits and 256 cells attached to each bitline. It is targeted to work at the supply voltage ranging from 0.3 V to 0.6 V. The architecture of adiabatic SRAM design is shown in Figure 3.
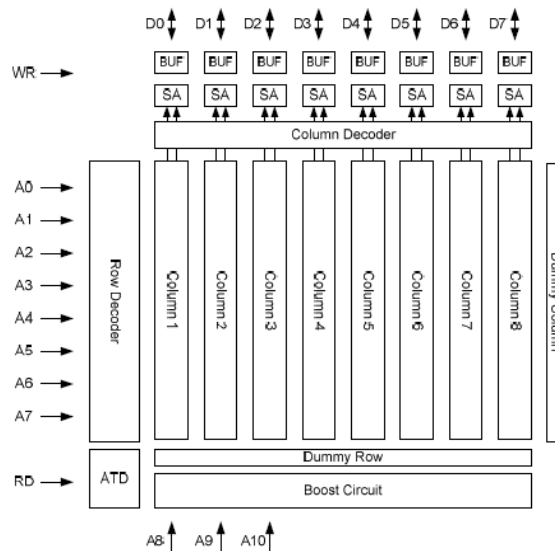

Figure 3: Architecture of proposed Adiabatic SRAM

There are 8 row address inputs (A0-A7) and 3 column address IOs (A8-A10), 8 bidirectional data IOs (D0-D7), as well as read (RD) and write (WR) enable signal inputs. There are two major parts of this ADIABATIC SRAM chip, the memory core and periphery circuits. The memory core contains the cell array, dummy column, dummy row, sense amplifiers and boost circuit. Their names and functions are

listed as follows. The designed SRAM was simulated and compared with 6T conventional and 7T SRAM cell for power consumption.
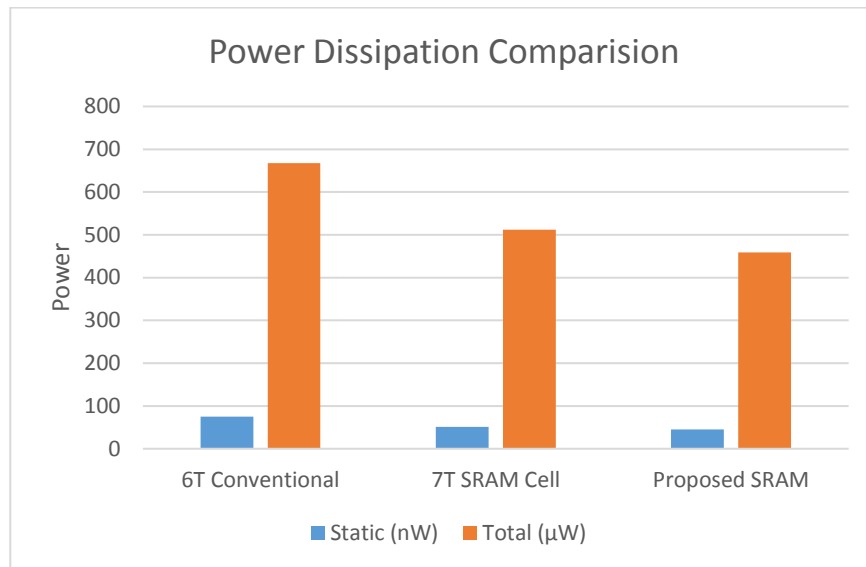

Figure 4: Power dissipation comparision

From the simulation results it is evident that the power dissipation of the designed adiabatic SRAM is 25% lower than conventional 6T SRAM whereas the power dissipation is approximately 15% lower than 7T CMOS SRAM. Figure 3 shows the comparative analysis of the 6T conventional SRAM, 7T CMOS SRAM & Proposed adiabatic SRAM.

VI. CONCLUSION

We have demonstrated a novel application of the principle of adiabatic switching to the design of SRAM, which can be implemented without significantly increasing area or circuit, complexity. Our design also provides the flexibility for possible optimizations of the SRAM from overall architectural considerations. Results indicate that the essential advantage of adiabatic logic, that of low-power, is achievable in SRAM.

VII. FUTURE WORK

This research contributes to better understanding of energy recovery SRAM. This work showed that the total energy and the energy during write cycle in particular will be saved in the proposed Adiabatic SRAM.

1. The investigations reported in this work are for moderate memory size. However if bigger memories are to be realized, one has to look into memory organization problem from the point of writing, reading and hold mode.
2. Further new topologies for SRAM cells and bit line architectures should be explored to minimize the energy consumption.
3. The design approach can be done at abstract level. Analytical models for energy consumption in deep submicron technology SRAMs and those for performance parameters should be developed so that optimization of one can be done with respect to the other.

ACKNOWLEDGEMENT

REFERENCES

[1]. Anantha P. Chandrakasan, Robert W. Brodersen, "Low Power Digital CMOS Design", Kulwer Academic Publishers, 2002.

[2]. Michael P. Frank and Marco Ottavi, "Energy Transfer and Recovery Efficiencies for Adiabatic Charging with various driving waveforms," Research Memo, 2006.

[3]. Maojiao He, Michael P. Frank, HuikaiXie, "CMOS-MEMS Resonator as a Signal Generator for Fully-Adiabatic Logic Circuits", Proceedings of SPIE, vol. #5649, paper #18, 2010.

[4]. Philip Teichmann, "Adiabatic Logic: Future trends and system level perspective", Springer, 2012.

[5]. Nakata, S., Honda, R., Makino, H., Mutoh, S., Miyama, M., Matsuda, Y., "General Stability of Stepwise Waveform of an Adiabatic Charge Recycling Circuit With Any Circuit Topology," IEEE Transactions on Circuits and Systems I: Regular Papers, vol.59, no.10, pp.2301-2314, Oct. 2012. doi: 10.1109/TCSI.2012.2189054

[6]. Reddy, N.S.S., Satyam, M., Kishore, K.L., "Cascadable adiabatic logic circuits for low-power applications," Circuits, Devices & Systems, IET , vol.2, no.6, pp.518-526, December 2008. doi: 10.1049/iet-cds:20080106

[7]. Michael P. Frank, "Common mistakes in adiabatic logic design and how to avoid them," Proceedings of the International Conference on Embedded Systems and Applications, held in Las Vegas, Nevada on June 23-26, 2003, pp. 216-222, CSREA Press.

[8]. Sergei Skorobogatov, "Low temperature data remanence in static RAM", Technical reports, Computer Laboratory, University of Cambridge, Number 536, June 2002.

[9]. Kulkarni, J.P.; Keejong Kim; Roy, K., "A 160 mV Robust Schmitt Trigger Based Subthreshold SRAM," in Solid-State Circuits, IEEE Journal of , vol.42, no.10, pp.2303-2313, Oct. 2007.

[10]. Kosonocky, Stephen V., Bhavnagarwala, Azeez , "Quasi-static random access memory", International Business Machines Corporation, United States Patent 6975532.

[11]. Preston, Ronald P., "14: Register Files and Caches", The Design of High Performance Microprocessor Circuits. IEEE Press. p. 290.

[12]. Upadhyay, P.; Mehra, R.; Thakur, N., "Low power design of an SRAM cell for portable devices," in Computer and Communication Technology (ICCCT), 2010 International Conference on , vol., no., pp.255-259, 17-19 Sept. 2010.

[13]. Ye, Yibin; Somasekhar, Dinesh; and Roy, Kaushik, "On The Design of Adiabatic SRAMs" (1996). ECE Technical Reports. Paper 104.

[14]. Jianping Hu; Xu, Tiefeng; Junjun Yu; Yinshui Xia, "Low power dual transmission gate adiabatic logic circuits and design of SRAM," in Circuits and Systems, 2004. MWSCAS '04. The 2004 47th Midwest Symposium on , vol.1, no., pp.I-565-8 vol.1, 25-28 July 2004.

[15]. Jun-Jun Yu; Peng-Jun Wang, "Design of Adiabatic SRAM Based on CTGAL Circuit," in Solid-State and Integrated Circuit Technology, 2006. ICSICT '06. 8th International Conference on , vol., no., pp.2118-2120, 23-26 Oct. 2006.

[16]. Sunil Jadav, Vikrant, Munish Vashisath, "Design and Performance Analysis of Ultra Low Power 6T SRAM using Adiabatic Technique", International Journal of VLSI design & Communication Systems (VLSICS) Vol.3, No.3, June 2012.

[17]. Ankita Singh, Vishal Moyal, "An Adiabatic 8T SRAM", International Journal of Advanced Research in Computer Engineering & Technology (IJARCET) Volume 3 Issue 8, August 2014.

[18]. Poonam Boora, Ramnish Kumar, "Performance Analysis of Adiabatic 6T SRAM and Bulk-Biased 6T SRAM", International Journal of Electronics & Communication Technology, Vol. 6, Issue 3, July - Sept 2015.

[19]. R. Sindhu, Shivani Patel, P.Ram Mohan Rao, "Single Ended SRAM Array Design Using NBTI Technique", International Journal & Magazine of Engineering, Technology, Management and Research, Volume No: 2, Issue No: 6, June 2015

[20]. Sriramoju Nagarani, Rayabarapu Venkateshwarlu, "A Novel 6T SRAM Based Design with Integration of NBTI Technique", International Journal of Engineering & Science Research, Vol-5, Issue-6, pp. 411-414, June 2015.

[21]. Nikita V. Keche, Ashish E. Bhande, "A Survey on Design of Efficient Nonvolatile SRAM Cell for Instant On-Off Operation", International Journal of Engineering Research and General Science Volume 3, Issue 2, Part 2, March-April, 2015.

[22]. Weiqiang Zhang, Beibei Qi, Jianping Hu and Jianhui Lin, "Super-Threshold Adiabatic SRAM Based On PAL-2N Operating In Medium Strong Inversion Region", International Journal of Control and Automation Vol.8, No.8, pp.17-26, 2015.

[23]. Santhiya.V, Mathan.N, "Review on Performance of Static Random Access Memory (SRAM)", International Journal of Advanced Research in Computer and Communication Engineering Vol. 4, Issue 2, February 2015.

[24]. Priyanka Ojha, Charu Rana, "Design of Low Power Sequential Circuit by using Adiabatic Techniques", I.J. Intelligent Systems and Applications, 08, 45-50, July 2015.

[25]. Saravanan.S, Senthil Kumar.V.M, Kavipriya.R, Devika.R, Divya.S, Gowri Shankari.G.K, "IG-FinFET Based 6T-SRAM Design Using SVL Technique", International Journal of Innovative Research in Science, Engineering and Technology, Vol. 4, Special Issue 6, pp. 445-452, May 2015.

AUTHORS BIOGRAPHY

Amit Saxena has 12 Years of experience in the field of Academic. He started his career from MIT, Moradabad. Presently he is working as an Assistant Professor, Deptt of E&C Engg., at MIT Moradabad. He obtained his Bachelor's degree in Electronics & Communication Engineering from I.E.T., Rohilkhand University, Bareilly and Masters degree (VLSI Design) in 2009 from UPTU, Lucknow. He is currently pursuing Ph.D. from Monad University Hapur. He has published number of papers in international & national journals, conferences and seminars.

Kshitij Shinghal has 16 Years of experience in the field of Academic and is actively involved in research & development activities. He obtained his Doctorate degree from UPTU, Lucknow in 2013, Masters degree (Digital Communication) in 2006 from UPTU, Lucknow. He started his career from MIT, Moradabad. Presently he is working as an Associate Professor & Head, Deptt of E&C Engg., at MIT Moradabad. He has published number of papers in national journals, conferences and seminars. He has guided two Masters, more than sixty students of B. Tech, and guiding three Ph.D. & M. Tech. theses. He is an active Member of Various Professional Societies such as ISTE, IACSIT, IAENG etc.

Deepti Shinghal was born in Moradabad, Uttar Pradesh, India in January 1980. She received her Bachelor of Engineering (B.E.) degree in Electronics and Communication Engineering Rohilkhand University, Bareilly in 2000. Thereafter she worked for one year as a Faculty Member in the Department of Electronics and Communication Engineering at Aligarh Institute of Engineering & Technology, Aligarh. Then she joined the Moradabad Institute of Technology, Moradabad in 2002. She received her M. Tech. degree in VLSI Design from U. P. Technical University, Lucknow in the year 2008. She is pursuing Ph.D. from Monad University Hapur.