International Journal of Engineering Sciences & Emerging Technologies, Oct. 2023.
ISSN: 22316604 Volume 11, Issue 2, pp: 323-326 ©IJESET

LOW LEAKAGE ADAPTIVE BIASING SCHEME FOR SRAM

Manas Singhal

Assistant Professor, Department of ECE,
Moradabad Institute of Technology, Moradabad, UP, India
Manas.singhal.ec@gmail.com

ABSTRACT

In this paper a technique that consumes low power for SRAM is proposed. It is achieved by reducing the leakage current in SRAM, this is achieved by using optimum level of source voltage of each individual fine-tuned memory block, while achieving the lower power levels the data is also securely stored during standby stage in each individual memory block. In traditional methods a uniform source voltage was applied to each block of memory but here the available memory is divided into different blocks and the different supply voltage is provided to an individual block after fine tuning. By determining and providing optimum voltage the leakage current is minimized.

KEYWORDS: *SRAM, Leakage Current, Power consumption*.

1. INTRODUCTION

Four transistors are used to store single bit in an SRAM. Each pair of transistor a cross-coupled inverter as shown in Fig. 1. There are two stable states of this cell. These states are denoted with 0 and 1. During the operations of read and write the access to a storage cell is controlled by the *access* transistors. Cell access is provided by Word line (WL). Word line (WL) transfer data in read and write operations. There is no strict requirement of two bit lines, but having two bit lines improves the noise margins.

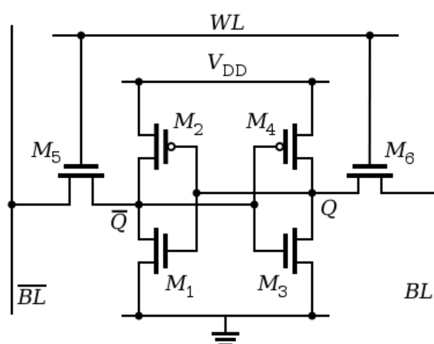

Fig. 1: SRAM cell

2. SRAM OPERATION

There are three different states of an SRAM cell. These three states are

- *Standby state: In this state the circuit remains idle*,
- *Reading* State: *In this state the circuit* request the data and

- *Writing* State: *In this state the circuit* update the data.

The word line must be asserted to connect the cell from the bit lines by using transistors M5 and M6. M1 – M4, connected to power supply, forms the cross-coupled inverter.

Read Operation of SRAM: Read Operation of SRAM is shown in Fig. 2.

- Assume Q=1. Set the bit lines to logic 1, Set WL, values stored in Q and Q' are transferred to the bit lines by leaving BL at 1 and discharging BL' to a logical 0 .
- If Q= 0, BL will be set to 1 and BL' to 0. The sense amplifier determines the line having higher voltage and thus decide in favor of 1 or 0. The speed of read operation can be increased by increasing the sensitivity of sense amplifier.

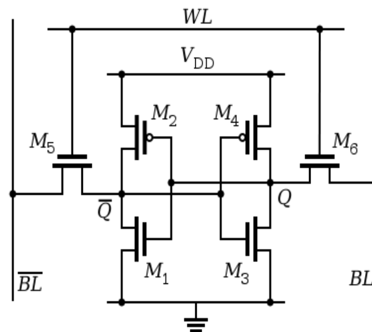

Fig. 2: Read Operation of SRAM

Write Operation of SRAM: Write Operation of SRAM is shown in Fig. 3. The value that is to be stored is provided on the bit lines. If we wish to write a 0, Set BL to 0 and BL' to 1. By setting BL to 1 and BL' to 0 1 can be written. WL is then asserted. Bit line input-drivers override the cross-coupled inverters previous state, it is possible only due to the fact that the transistors used are relatively weak when compared to bit-lines input drivers. .

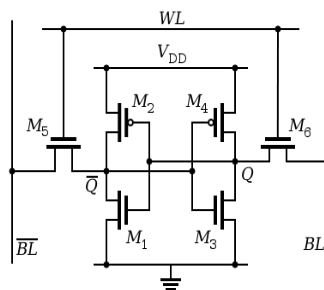

Fig. 3: Write Operation of SRAM

3. LEAKAGE POWER AND SUB-THRESHOLD LEAKAGE CURRENT IN SRAM

There are two main components of power dissipation in CMOS circuits. First is Static power dissipation and the other is dynamic power dissipation.

Charging of load capacitances and discharging of load capacitances mainly results in Dynamic dissipation. The current is constantly drawn from the power supply, which results in Static dissipation. Sub-threshold leakage current is the main contributor of leakage. The low leakage SRAM is shown in figure 4.

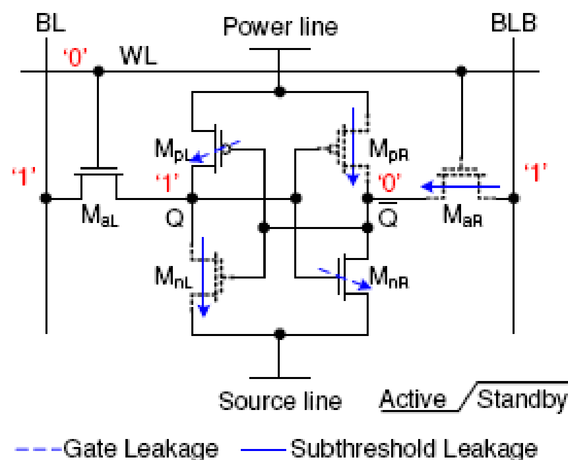

Fig. 4: Low leakage SRAM

The current that flows from drain to source even when the transistor is off is termed as Subthreshold leakage current and it can be given as follows

$$I_{Dsub} = I_{s0} \cdot [1 - e^{\frac{-V_{ds}}{V_t}}] \cdot [e^{\frac{V_{gs} - V_T - V_{off}}{nV_t}}]$$

Equation shows the sub threshold drain current.

V_{off} - model parameter,

I_{s0} - current dependent on the transistor geometry

n - device parameters,

4. RESULTS

The distribution of voltage supply after fine tuning results in the reduction of the leakage current, which in turn increases the power efficiency of the presented SRAM device.

5. CONCLUSION

This paper propose a technique that consumes low power in SRAM, this is achieved by using optimum level of supply to each individual fine-tuned memory block, while achieving the lower power levels the data is also securely stored during standby stage in each individual memory block. In traditional methods a constant voltage was applied to each block of memory but here the available memory is divided into different blocks and the different supply voltage is provided to an individual block after fine tuning. By determining and providing optimum voltage the leakage current is minimized.

REFERENCES

[1]. H. Mizuno and T. Nagano, “Driving source-line cell architecture for sub-1-v high-speed low-power applications,” IEEE Journal of Solid-State Circuits, vol. 31, no. 4, April 1996.

[2]. A. Agarwal, H. Li, and K. Roy, “A single-Vt low-leakage gated-ground cache for deep submicron,” IEEE Journal of Solid State Circuits, vol. 38, no. 2, pp. 319–328, Feb. 2003.

[3]. K. Zhang, U. Bhattacharya, C. Zhanping, F. Hamzaoglu, D. Murray, N. Vallepalli, W. Yih, B. Zheng, and M. Bohr, “SRAM design on 65-nm CMOS technology with dynamic sleep transistor for leakage reduction,” IEEE Journal of Solid State Circuits, vol. 40, no. 4, pp. 895–901, April 2005.

[4]. M. Khellah, N. S. Kim, J. Howard, G. Ruhl, M. Sunna, Y. Ye, J. Tschanz, D. Somasekhar, N. Borkar, F. Hamzaoglu, G. Pandya, A. Farhang, K. Zhang, and V. De, “A 4.2GHz 0.3mm2 256kb

dual-Vcc SRAM building block in 65nm CMOS," in Proc. of IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers, Feb. 2006, pp. 5–7.

[5]. E. S. Sr., F. J. List, and J. Lohstroh, "Static-noise margin analysis of MOS SRAM cells," IEEE Journal of Solid-State Circuits, vol. 22, no. 4, pp. 748–754, October 1987.

[6]. Berkeley Predictive Technology Model. [Online]. Available: http://www-device.eecs.berkeley.edu/∼ptm

[7]. A. Agarwal, D. Blaauw, and V. Zolotov, "Statistical timing analysis for intra-die process variations with spatial correlations," (ICCAD), November 2003, pp. 900–907.