EFFECT OF CHANNEL THICKNESS ON THE PROPERTIES OF METAL SEMICONDUCTOR FIELD EFFECT TRANSISTOR

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ABSTRACT

The drain characteristics of metal-semiconductor thin film transistors have been investigated. It consists of a metal contact layer and a semiconducting layer, which forms metal-semiconductor junction. The top gated metal layer is deposited for conduction of charge carriers which flows from source to drain and controlled with Schottky metal gate. The channel control has been obtained by varying the width of depletion layer by depositing different thickness of conducting channel of selenium layer and the flow of current between source and drain. The films have been studied for their structural and electrical properties. The metal gate electrodes have been directly deposited on the selenium channel without any insulating layer, because of the formation of Schottky barrier at the interface of metal and semiconductor.

KEYWORDS—*Metal Semiconductor Field Effect, Thermal evaporation, schottky metal gate Introduction*

I. Introduction

Thin films deposition increased with the contact area of the cell components, which results in high fraction reactants. Thin films have high current density and cell efficiency obtained due to the transportation of ions throughout thin-film layers as compared to bulk materials. Metal-semiconductor thin film deposition is interesting property in the era of miniaturization of electronic and chemical components. Materials of different thicknesses have been used to vary the physical and electrical properties which depend on the nature of the material which gives considerable functional applications of electronic device application and different physical properties, when it combines with different materials [1]. The metals show high conductivity and being used to increase the electrical resistivity and sheet resistance with a decrease in thickness by highly scattered free electrons, so conductivity has increased with increased thicknesses of thin film [2]. These results have been used for electronic devices and microelectronic industry applications. Thickness plays a very important role to observe the properties of metals [3]. The reactively sputtered Schottky contact on ZnO single crystal includes electrical properties of thin film conduction and I-V characterization by varying thickness temperature and current density [4].Selenium is a metalloid it has some characteristics of metal & some characteristics of non metal so it is also called as semiconductor. dissimilar metal-semiconductor-metal ratios results by evaporation of after heating in a vacuum chamber, resting on the confidence of size of crystallite, orientation preferential, unevenness, have been studied, In metal semiconductor interface gate made by metal forms a schottky barrier will be formed [5]. The free electrons are able to cross the depletion region with effect of energy source from one side to other. Source and drain are directly connected to semiconductor, determine transistor dimensions. Aluminum is used as contact material in IC's exhibits good corrosion resistance. As voltage which has applied to gate electrode bulk charge is involved with electric field applied which structure conducting channel. Glass plate is used as a substrate on which active layer is grown to make it partially insulating substrate. The higher transit frequency of the FET has common application in microwave circuits [6].

II. Experimental

The samples had equipped by thermal evaporation at a pressure of 10^{-5} torr. High purity of Aluminium sheet and Copper about 99×999% pure, and selenium Powder purchased from Koch-Light laboratories LTD, colnbrook Berks England [7]. The properly cleaned glass substrate of 1x1 cm^2 dimension, substrate cleaning is done using soap solution and keeps it in hot chromic acid and then cleaning done by deionized water then rinse in acetone, were placed in the holder situated above the tungsten boat which carrying materials. After reaching the high vacuum (10^{-5}torr) in the chamber the metal and Se heated by transient the current slowly to the electrodes [8].Selenium having thicknesses 1000 Å was first evaporated and later metal of constant thickness (500 Å) deposited over these films to get metal–Se bilayer structure. Thickness of the material on substrate was controlled using quartz crystal monitor (“Hind Hivac” Digital Thickness Monitor Model–DTM–101) [9]. Metal having thicknesses 500 Å were again evaporated at high pressure and deposited on bilayer structure to form a trilayer metal gate contact for thin film structure. The total thickness of the Metal-Se-Metal thin film is about 200 nm and the thickness of a single layer is 50 nm/100 nm/50 nm.

III. Results And Discussion

Electrical properties

It has observed that the fabricated FET is gives the increase of the drain current at negative gate voltages of a MESFET (between 0 V to 5 V) and which has compared to quadratic expression [10].

$$I_{D,sat} = \mu_n \frac{\varepsilon_s}{w} \frac{W}{L} \frac{(V_G - V_T)^2}{2} \quad (3.1)$$

Where w is the width of depletion layer in channel layer [8]. The quadratic expression given as

$$V_G = \emptyset_i \text{ for } w = 3d/8 \quad (3.2)$$

The gate – channel built in potential is given by

$$V_{bi} = \emptyset_m - [\chi + \frac{t_g}{2q} - \frac{k_B T}{q} \ln\left(\frac{N_D}{n_i}\right)] \quad (3.3)$$

The metal semiconductor junction at the gate is sufficient to deplete the entire channel region [8].Hence the conduction channel is absent at Vgs =0 V. So such devices are constructed by incorporating a very thin epitaxial layer on semi-insulating substrate, using a semiconductor like selenium [11].Drain characteristics for the typical Field Effect Transistor is shown in Fig 1 at various gate to source fixed voltages. Fabricated MESFET using metal contact of aluminum is shown in Fig 2.The basic shape of curve is similar for the normal field effect transistor. MESFET requires positive gate voltages to allow reasonable gate currents. To an extent, the channel conductivity can be increased by increasing the channel carrier concentration [7].The individual graphs between drain current and drain voltage are shown in fig. 3 at (a) VGS =1V (b) VGS=3V(C) VGS=5V as the Drain characteristics of MESFET using Aluminum as Metal contact.

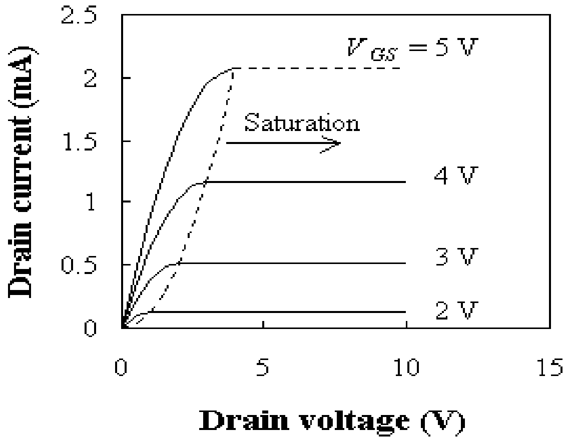


Figure 1: Typical Drain Characteristics of FET

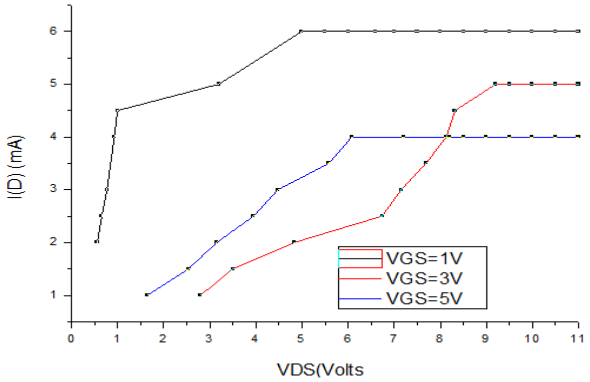
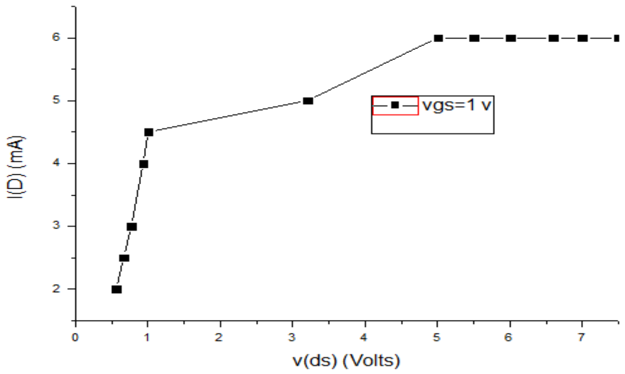


Figure 2: Graph between drain current and drain voltage as the Drain characteristics of MESFET using Aluminum



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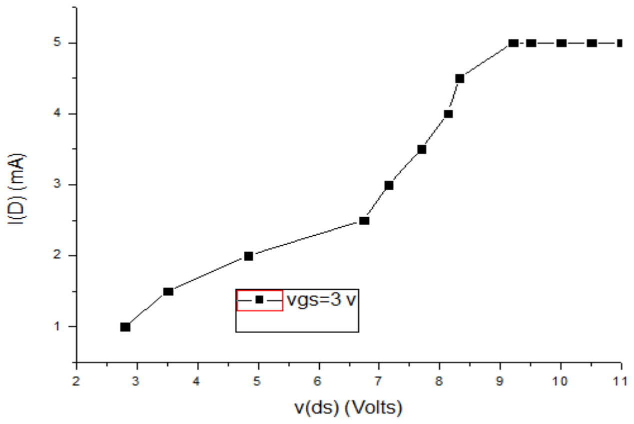

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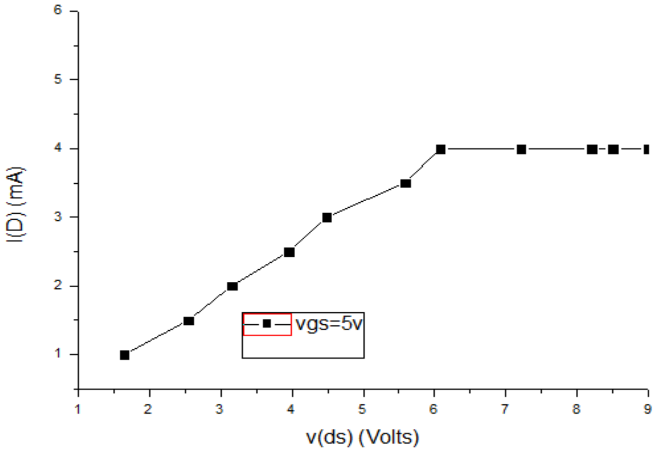

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Figure 3: Graph between drain current and drain voltage at (a) V_{GS} =1V (b) V_{GS}=3V(C) V_{GS}=5V as the Drain characteristics of MESFET using Aluminum as Metal contact

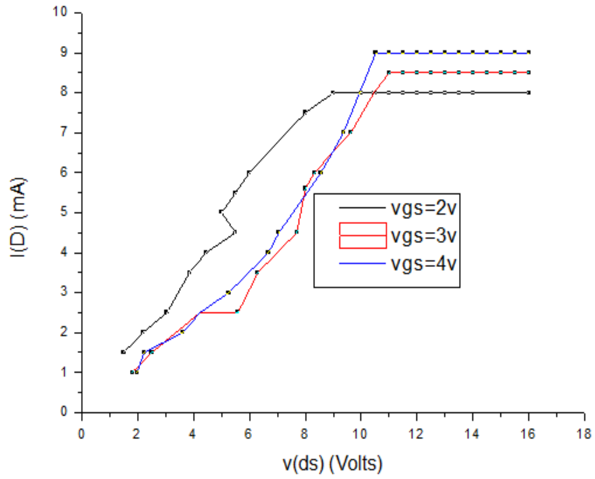
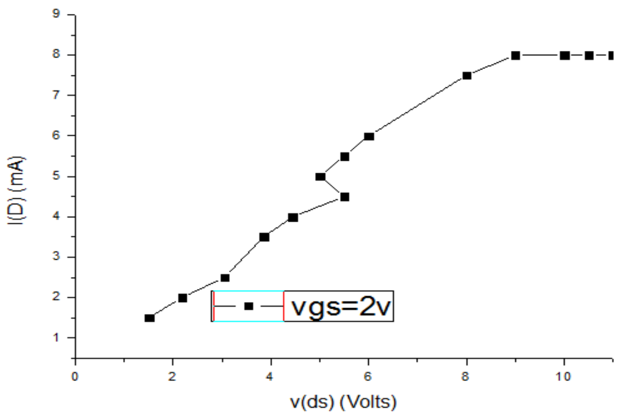
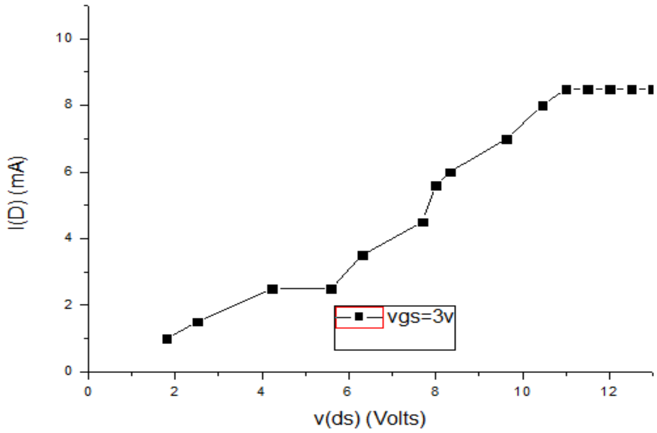


Figure 4: Graph between drain current and drain voltage as the Drain characteristics of MESFET using Copper as Metal contact



(a)



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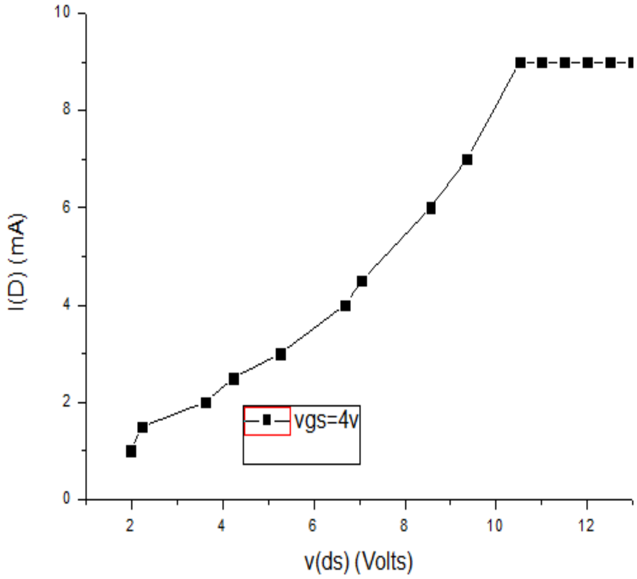


(C)

Figure 5: Graph between drain current and drain voltage at (a) V_{GS} =2V (b) V_{GS}=3V(C) V_{GS}=4V as the Drain characteristics of MESFET using Copper as Metal contact

Fig. 4 gives the graph between drain current and drain voltage as the Drain characteristics of MESFET using Copper as Metal contact and Fig. 5 shows the individual graphs of drain characteristics at different V_{GS}. The investigation shows FET was work as that straight MOSFET but flow of carrier from source to drain has controlled with schottky top metal gate. By varying the width of depletion layer channel has controlled using metal contact which modulates the thickness of conducting channel which causes flow of current between source and drain. [11, 12].

Table 1 MESFET Fabrication Parameters

Parameter	Symbol	Value	
Channel width	W	3 mm	3 mm
Channel length	L	14 mm	14 mm
Channel doping	Nd	1017 cm-3	1017 cm-3
Channel thickness	D	630 nm	300 nm
Pinch off Voltage	Vp	3.5*10-3 V	8.1*10-3 V
Built-in potential	ϕI	1 V	1.6 V

Investigation gives results that the flow of charge carrier is from source to drain which is control by Schottky metal gate. By the depletion layer variation, channel width has controlled by the metal contact and thickness of the conducting channel (selenium channel) controlled by current from source to drain.

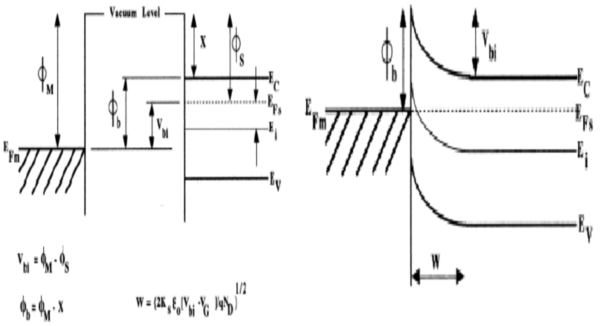


Fig.6 The energy band diagram of Schottky contact

The Schottky contact is formed when a metal and semiconductor are in intimate contact and the work function of the metal Φm is larger than the work function of the semiconductors [13,14]. When there is a contact, a potential barrier of height Φm has been formed between the metal and the semiconductor, which equals to the work function of the metal minus the electron affinity (χ) of the semiconductor [15].A built-in potential V_{bi}, has been created at a Schottky contact due to a misalignment in the Fermi energies of metal and the semiconductor [16]. Typically, the work function of the metal is greater than that of an n-type semiconductor, and the semiconductor valence and conduction bands will bend upward at the inference in order to align the Fermi levels [17]. The amount that the energy bands bend upwards at the interface is known as the built-in potential V_{bi}. The relation of these parameters is shown in Fig.6.

Structural Properties of the thin film

XRD Analysis

The thin film structural properties characterized using XRD pattern in Fig 7.It shows corresponding XRD peaks for copper and selenium at exact 2θ angle equivalent to the orthorhombic face of thin film. In This work it has been analyze that Cu and Se has deposited on glass substrate.

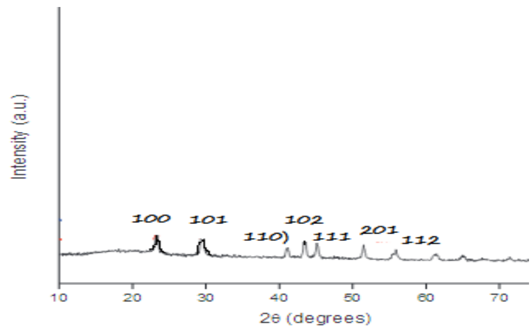


Figure 7: XRD for thin films as prepared

Similarly when Al and Se are as deposited on glass substrate shown in Fig 8, all peaks of Al and Se are shown in XRD. The films deposited at RT and annealed at 50°C, 100°C are amorphous.

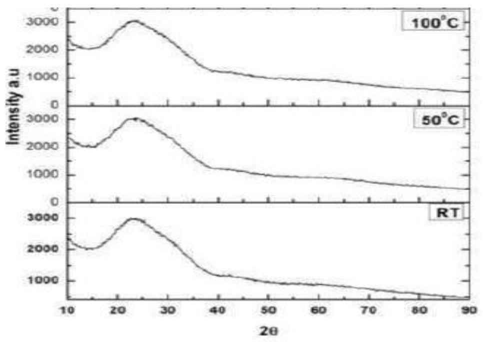


Figure 8: XRD for aluminum selenide thin films prepared at RT, Annealed at 50°C, 100°C

Atomic Force Microscopy (AFM)

Three layers of material were deposited on glass substrate and form the junction.

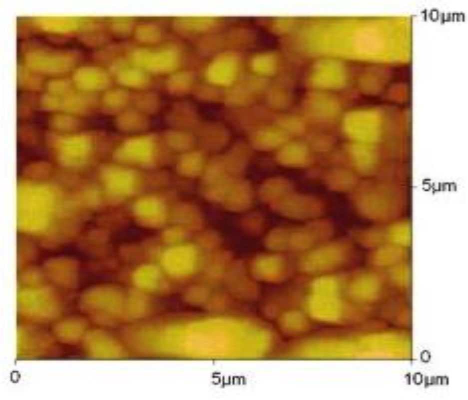
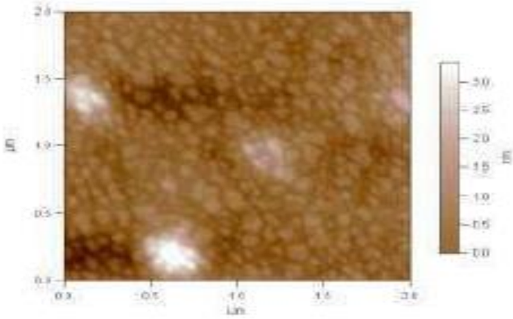
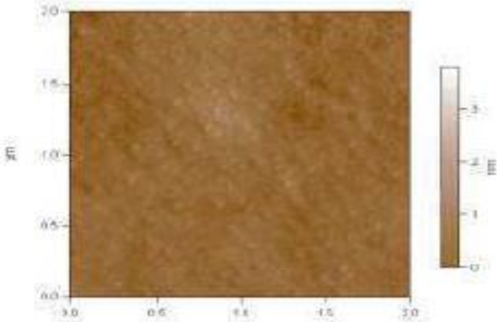


Figure 9: AFM images of film

The surface morphology of the as deposited and annealed films was studied with the help of Atomic Force Micrographs. The samples were scanned for 2 × 2 µm^2 area shown in fig 10 for RT, Annealed at 100°C.



(a)



(b)

Figure 10: AFM images of aluminum selenide thin film (a) room temperature (b) 100°C annealing

Scanning Electron Microscopy (SEM)

Plane morphology of thin films in Fig 11 shows the morphology of the Cu-Se thin films. Holes on the surface of the film appeared because of the film are as deposited [18].

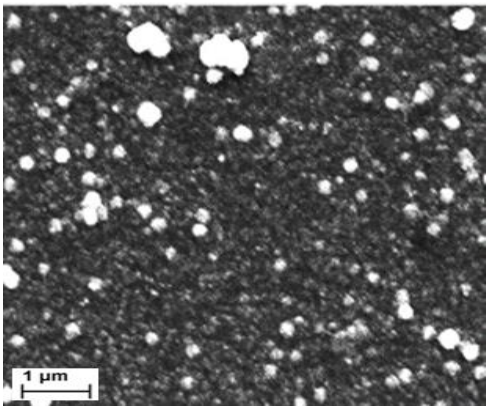
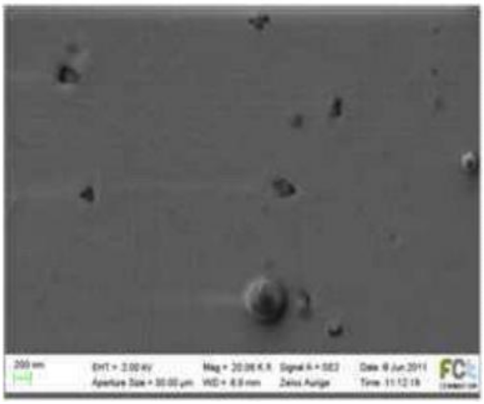
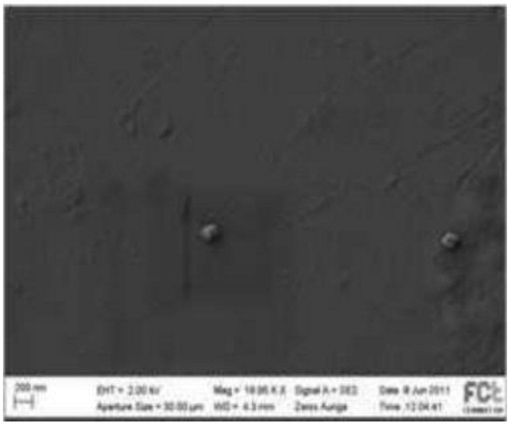


Figure 11: SEM micrographs of thin films



(a)



(b)

Figure 12: SEM micrographs of aluminium selenide thin films (a) prepared at RT (b) annealed at 50°C

Surface morphology of aluminium selenide thin films. In Fig.12 shows that the annealing process modifies the morphology of the holes on the surface of the film at RT disappeared due to annealing at 50°C [19, 20].

IV. Conclusion

This research has been done for obtaining the better device performance by using the selenium material as semiconductor in MESFET. By using different device parameters better results have been obtained for threshold voltage. To enhance and optimize the performance sustainable and alternative semiconductors have been used of TFT in terms of composition and structure of materials. The additional important parameter is methods of deposition.TFT are also fabricated by using different stacked structure by depositing the different layer of materials on the substrate. We demonstrate the experimental research investigations on a Thin Film Transistor for the application of Metal semiconductor field-effect transistor. Metal and Metalloid fabricated on the glass substrate as thin film samples and electrical behavior has been found similar to Thin Film Field Effect Transistor. The majority carriers flow from source to drain with the conducting semiconductor layer of selenium and control of charge has been done by schottky metal gate formed at metal semiconductor junction. Metal (Al/Cu) contact and metalloid (Se) channel has been used as a Field Effect Transistor on a glass substrate by depositing the source, drain and top-gate metal contacts. The thickness of thin Film ~200 nm, The source and drain of the FET structure were defined by the metal layers Al/Cu (100-nm) were sequentially deposited on the Se in the defined contact patterns by Thermal evaporation. The thin films were deposited from synthesized nanoparticles and were annealed at different temperature (50°C, 100°C) for 20 minutes under a low vacuum its electrical properties have characterized.

V. Future Scope

Device fabrication such as transparent resistive random access memory (TRRAM), solar cell, Light emitting diode etc. Multilayer study of various material thin films of various thicknesses using the different substrate. Selenium-based nanocrystalline thin films using another advanced technique ex. PLD, RF –Sputtering etc.

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