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CONCURRENT FAULT RECTIFICATION (CFR) ARCHITECTURE FOR MOTION ANALYSIS COMPUTING ARRAYS

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ABSTRACT
This paper develops a novel Concurrent Fault Rectification (CFR) architecture for Motion Analysis Computing Arrays (MACA). Any single fault in each Processing Element (PE) in an MACA can be effectively detected and corrected using the concept of Dual-Remnant codes i.e., Remnant and Proportionate (RP) code. A Good Example is the H.264 video compression standard, also known as MPEG-4 Advanced Video Coding application. It uses a context-based adaptive method to speed up the multiple reference frames Motion Analysis by avoiding 76%–96% unnecessary reference frames computation. A large PE array accelerates the computation speed especially in High Resolution devices such as HDTV(High Definition Television).The Visual Quality and Peak Signal-to-Noise Ratio (PSNR) at a given bit rate are influenced if a fault occurred in MA process.

KEYWORDS – *motion analysis, fault rectification, remnant and proportionate code, processing element.*

I. INTRODUCTION

Improved advancements in semiconductors, digital signal processing, and communication technologies have made multimedia applications more flexible and reliable. A good example is the H.264 or MPEG-4 Part 10 Advanced Video Coding, which is the next generation video compression that is necessary for a wide range of applications to reduce the total data amount required for transmitting or storing video data. Among the coding trends, a MA is of high importance in exploiting the temporal redundancy between subsequent frames that provides the less computation time for coding. Moreover, while performing up to 76%–96% of the computations encountered in the entire coding system, a MA is widely regarded as the most computationally intensive of a video coding system. A MA generally consists of PEs with a size of NxN. Thus, increasing the speed of manipulation towards a high dimension of PE array, particularly in devices having more resolution factor with a large as N=4 for HDTV (High Definition Television) search range. Also, the video quality and peak signal-to-noise ratio (PSNR) are influenced for a given bit rate if a fault obtained in MA process. A testable design is thus increasingly important to ensure the reliability of numerous PEs in a MA. Moreover, although the advance of VLSI technologies facilitate the integration of a large number of PEs of a MA into every chip, the logic-per-pin ratio is consistently increased, thereby slightly decreasing the logic testing efficiency on the chip. For the commercial purpose, it is mandatory for the MA to enhance Design For Testability (DFT). DFT concentrates on improving the usage of testing the devices, thus makes the system highly reliable. DFT techniques depend on circuit re-configuration during testing to enhance the features of testable nature. Hence Design For Testability methods improves the testability design of circuits. Due to recent trends in micron technologies and increasing complexity of electronic systems and circuits, the Built-In Self-Test (BIST) schemes have supremely become necessary in this modern digital universe.

II. OVERALL CFR SYSTEM

The conceptual view of the proposed CFR scheme, which comprises two major circuit designs, i.e. Fault Detection Circuit (FDC) and data recovery circuit (DRC), to identify faults and recover the corresponding data in a specific CUT. The test code generator (TCG) in Fig. utilizes the concepts of RP code to generate the corresponding test codes for fault identification and data recovery. In other words, the test codes from TCG and the primary output from CUT are delivered to FDC to determine whether the CUT has faults. DRC is in charge of recovering data from TCG. Additionally, a selector is enabled to export fault-free data or data-recovery results. Importantly, an array-based computing structure, such as MA, discrete cosine transform (DCT), iterative logic array (ILA), and finite impulse filter (FIR), is feasible for the proposed CFR scheme to identify faults and recover the corresponding data. In our proposed circuit the output will be gating in second clock cycle not a 22th clock cycle, because we change the RP block structure. Also the proposed CFR design for MA testing can identify faults and recover data with an acceptable area and time limit. Importantly, the proposed CFR design performs satisfactorily in terms of throughput and reliability for MA testing applications.

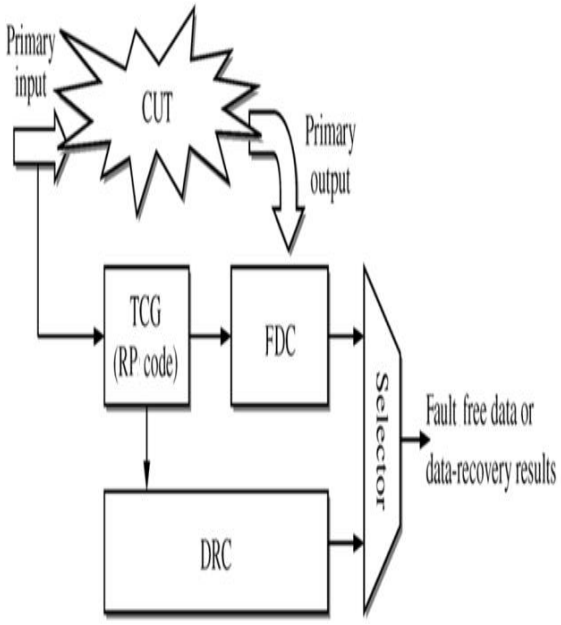

Fig.1. Block Diagram of CFR Process

Advantages in CFR System

1. More reliability and Throughput.
2. Less number of gate counts.
3. High Performance in terms of Operating Speed

III. MODULE DESCRIPTION

1. Processing Element

A MA (Motion Analysis) consists of many PEs incorporated in a 1-D or 2-D array for video encoding applications. A PE generally consists of two ADDs (i.e. an 8-b ADD and a 12-b ADD) and an accumulator (ACC). Next, the 8-b ADD (a pixel has 8-b data) is used to estimate the addition of the current pixel (Cur pixel) and reference pixel (Ref_pixel). Additionally, a 12-b ADD and an ACC are required to accumulate the results from the 8-b ADD in order to determine the sum of absolute difference (SAD) value for video encoding applications.

2. Sum of Absolute Difference Tree

We propose a 2-D intra-level architecture called the Propagate Partial SAD. This Architecture is composed of PE arrays with a 1-D adder tree in the vertical direction. Current pixels are stored in each PE, and two sets of continuous reference pixels in a row are broadcasted to PE arrays at the same

time. In each PE array of a adder tree, harmonics are identified and added by a adder tree to generate single row SAD. The row SADs are accumulated and propagated with propagation registers in the vertical direction. The reference data of searching candidates in the even and odd columns are inputted by Ref. Pixel 0 and Ref Pixel 1. Then the SAD of the initial search candidate in the zeroth column is generated, and the SADs of the other searching candidates are sequentially generated in the following cycles. When computing the last searching candidates in each column, the reference data of searching candidates in the next columns begin to be inputted by another input reference. While navigating in partial SAD, by sending reference pixel rows and also partial row SADs in the vertical scale direction, it gives the usage of lesser reference registers and a minimum critical path.

Sum of Absolute Difference Calculation:

By utilizing PEs, SAD shown in as follows, in a macro block with size N X N of can be evaluated:

$$\begin{aligned}\mathrm{SAD} &= \sum_{i=0}^{N-1}\sum_{j=0}^{N-1}|X_{ij}-Y_{ij}| \\ &= \sum_{i=0}^{N-1}\sum_{j=0}^{N-1}|(q_{xij}\cdot m+r_{xij})-(q_{yij}\cdot m+r_{yij})|\end{aligned}$$

Where $r_{xi,j}$,$q_{xi,j}$ and $r_{yi,j}$,$q_{yi,j}$ denote the corresponding RP code of $X_{i,j}$, $Y_{i,j}$ and modulo M. Importantly, and represent the luminance pixel value of Cur_pixel and Ref_pixel subsequently.

3. Remnant Proportionate Code Generation Algorithm

In this RPCG Algorithm Remnant code is generally separable arithmetic codes by estimating a remnant for data and appending it to data. Fault detection logic for operations is typically derived by a separate remnant code, making the detection logic is simple and easily implemented. Fault detection logic for operations is typically derived using a separate remnant code such that detection logic is simply and easily implemented. However, only a bit fault can be detected based on the remnant code. Additionally, a fault can't be recovered effectively by using the remnant codes. Therefore, this work presents a proportionate code, which is derived from the remnant code; to assist the remnant code in rectifying multiple

The corresponding circuit design of the RPCG is easily realized by using the simple adders (ADDs).Namely, the RP code can be generated with a low complexity and little hardware cost.

3. Test Code Generation

TCG is an important component of the proposed CFR architecture. Notably, TCG design is based on the ability of the RPCG circuit to generate corresponding test codes in order to identify faults and recover data.

4. Fault Detection Circuit

In this module indicates that the operations of fault detection in a specific PE_i is achieved by using FDC, which is utilized to compare the outputs between TCG and in order to determine whether faults have occurred. The FDC output is then used to generate a 0/1 signal to indicate that the tested PE_i is fault-free/faulty. Using XOR operation can be identify the fault if any variation in terms of remnant and proportionate value. Because a fault only affects the logic in the fan-out cone from the fault region. Concurrent fault simulation exploits this fact and simulates only the differential parts of the whole circuit Concurrent fault simulation is essentially an event-driven simulation with the fault-free circuit and faulty circuits simulated altogether.

5. Data Recovery Circuit

In this module will be generate fault free output by proportionate multiply with constant value and add with proportionate code. During data recovery, the circuit DRC plays a significant role in recovering RP code from TCG.

IV. METHODOLOGY

Coding approaches such as Parity code, Berger code, and Remnant code is considered only to identify circuit faults. Remnant code R is a separable arithmetic codes by estimating a remnant for data and appending it to data. i.e., $R = |X|_m$ .Binary Data X is coded as a pair (X,R) and modulus $m= 2^w -1$, w is word length. Proportionate code Q =X/m is derived from the Remnant code to identify and recover multiple faults. To simplify the complexity of circuit design, the implementation is carried out using the simple Adders (ADDs).

V. MODULE DIAGRAM

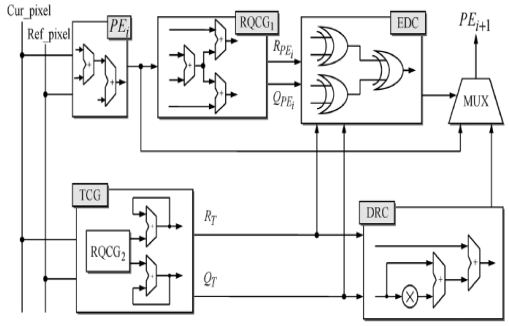

Fig.2. CFR design

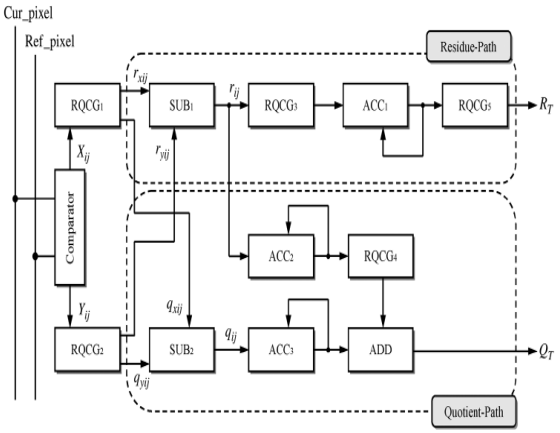

Fig.3. TCG design

VI. SIMULATION RESULTS

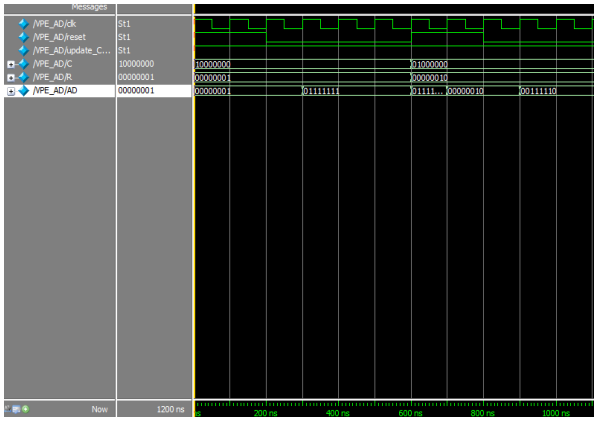

Fig.4. Processing element

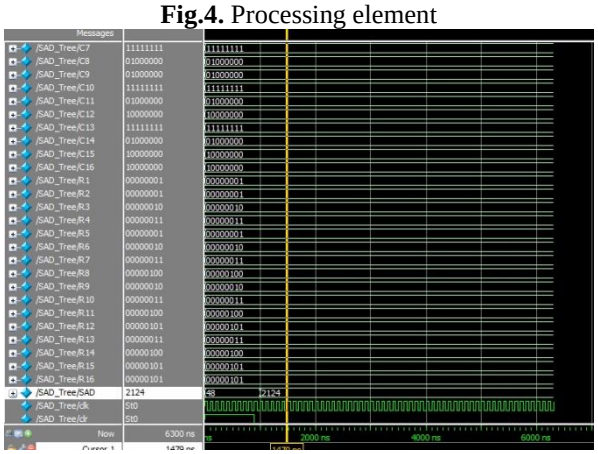

Fig.5. Sum of Absolute Difference Tree

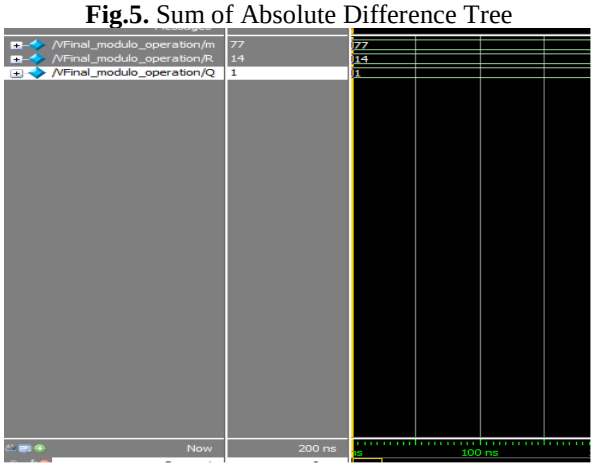

Fig.6. Remnant Proportionate Code Generation

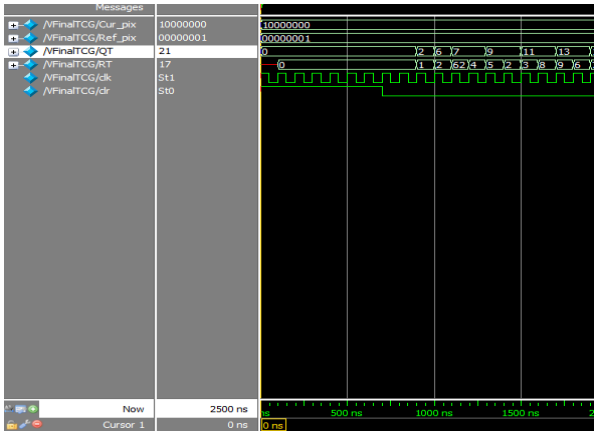

Fig.7. Test Code Generation

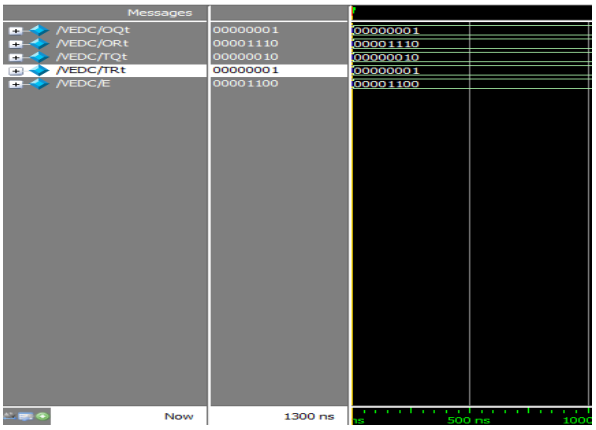

Fig.8. Fault Detection Circuit

Fig.9. Data Recovery Circuit

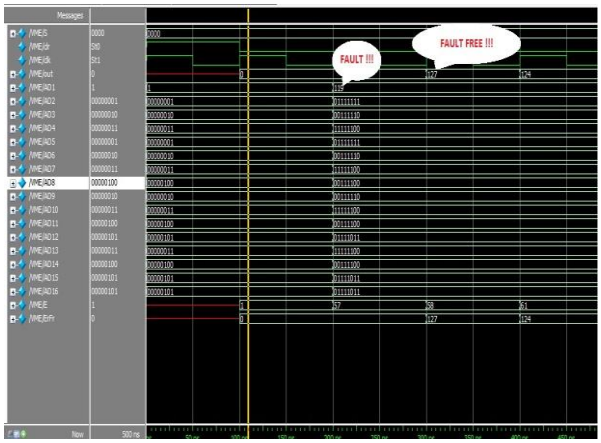

Fig.10. Overall CFR Process

VII. EXPERIMENTAL RESULTS

Table 1 Estimation Of Time Penalty for a specific PE in Overall CFR Process

Constraints	PE	RPCG	TCG	FDC	DRC
Operating time (μs)	0.97527	0.01017	1.01434	0.00514	0.01674
Time Penalty (%)		5.72%			

Time Penalty (%) = (TCG + DRC - PE) / PE * 100

= (1.01434 + 0. 01674 − 0.97527) / 0. 97527 * 100

= 5.72%

VIII. CONCLUSION

This work presents a novel CFR architecture for detecting the faults and recovering the data of PEs in a MA. Based on the RP code, a RPCG-based TCG design is developed to generate the corresponding test codes to identify faults and recover data. The CFR architecture is also implemented by using Verilog Hardware Description Language and synthesized by the synopsys Design Compiler with TSMC 0.18- m1P6MCMOS technology. Experimental results indicate that that the proposed CFR architecture can effectively identify faults and will recover data in PEs of a MA with reasonable less operating time of 5.72% with acceptable area overhead.

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