

INVESTIGATION OF FIVE-LEVEL CHB AS DISTRIBUTION STATIC COMPENSATOR (DSTATCOM) IN POWER SYSTEM (PS) FOR COMPENSATION OF REACTIVE POWER AND HARMONICS

Arun Kumar Rath¹, Srikant Misra¹, Ch. Venkateswra Rao²

¹Asst.Professor & ²Professor,

Electrical and Electronics Engineering, GIET, Gunupur, Odisha, India

rpmarun@gmail.com

ABSTRACT

With the widespread use of harmonic generating devices, the control of harmonic currents to maintain a high level of power quality is becoming increasingly important. An effective way for harmonic suppression is the harmonic compensation by using active power filter. This paper presents a comprehensive survey of DSTATCOM and is aimed at providing a broad perspective on the status of DSTATCOM control methods to researchers and application engineers dealing with harmonic suppression issues. Many control techniques have been designed, developed, and realized for active filters in recent years. This paper presents different types of Synchronous reference frame methods for real time generation of compensating current for harmonic mitigation and reactive power compensation. All the techniques are analyzed mathematically and simulation results are obtained which are being compared in terms of its compensation performance with different parameters under steady state condition. Shunt compensation for medium voltage distribution systems requires higher rating for voltage source converters (VSCs). Ratings of the semiconductor devices in a VSC are always limited; therefore, for higher rated converters it is desirable to distribute the stress among the number of devices using multilevel topology. Cascaded multilevel configuration of the inverter has the advantage of its simplicity and modularity over the configurations of the diode-clamped and flying capacitor multilevel inverters. Application of cascaded multilevel converters for shunt compensation of distribution systems has been described in Literature. This paper presents an investigation of five-Level Cascaded H – bridge (CHB) Inverter as Distribution Static Compensator (DSTATCOM) in Power System (PS) for compensation of reactive power and harmonics. The advantages of CHB inverter are low harmonic distortion, reduced number of switches and suppression of switching losses. A CHB Inverter is considered for shunt compensation of a 11 kV distribution system. Finally a level shifted PWM (LSPWM) and phase shifted PWM (PSPWM) techniques are adopted to investigate the performance of CHB Inverter. The results are obtained through Matlab/Simulink software package. The proposed DSTATCOM is simulated for both linear and nonlinear loads.

KEYWORDS- DSTATCOM, Power Quality Level shifted Pulse width modulation (LSPWM), Phase shifted Pulse width modulation (PSPWM), Proportional-Integral (PI) control.

I. INTRODUCTION

One of the most common power quality problems today is voltage dips. A voltage dip is a short time (10 ms to 1 minute) event during which a reduction in r.m.s voltage magnitude occurs. It is often set only by two parameters, depth/magnitude and duration. The voltage dip magnitude is ranged from 10% to 90% of nominal voltage (which corresponds to 90% to 10% remaining voltage) and with a duration from half a cycle to 1 min. In a three-phase system a voltage dip is by nature a three-phase phenomenon, which affects both the phase-to-ground and phase-to-phase voltages. A voltage dip is caused by a fault in the utility system, a fault within the customer's facility or a large increase of the load current, like starting a motor or transformer energizing. Typical faults are single-phase or multiple-phase short circuits, which leads to high currents. The high current results in a voltage drop over the network impedance. At the fault location the voltage in the faulted phases drops close to zero, whereas in the non-faulted phases it remains more or less unchanged [1, 2].

Voltage dips are one of the most occurring power quality problems. Of course, for an industry an outage is worse, than a voltage dip, but voltage dips occur more often and cause severe problems and economical losses. Utilities often focus on disturbances from end-user equipment as the main power quality problems. This is correct for many disturbances, flicker, harmonics, etc., but voltage dips mainly have their origin in the higher voltage levels. Faults due to lightning, is one of the most common causes to voltage dips on overhead lines. If the economical losses due to voltage dips are significant, mitigation actions can be profitable for the customer and even in some cases for the utility. Since there is no standard solution which will work for every site, each mitigation action must be carefully planned and evaluated. There are different ways to mitigate voltage dips, swell and interruptions in transmission and distribution systems. At present, a wide range of very flexible controllers, which capitalize on newly available power electronics components, are emerging for custom power applications [3, 4]. Among these, the distribution static compensator and the dynamic voltage restorer are most effective devices, both of them based on the VSC principle.

The STATCOM used in distribution systems is called DSTACOM (Distribution-STATCOM) and its configuration is the same, but with small modifications. It can exchange both active and reactive power with the distribution system by varying the amplitude and phase angle of the converter voltage with respect to the line terminal voltage.

A multilevel inverter can reduce the device voltage and the output harmonics by increasing the number of output voltage levels. There are several types of multilevel inverters: cascaded H-bridge (CHB), neutral point clamped, flying capacitor [2-5]. In particular, among these topologies, CHB inverters are being widely used because of their modularity and simplicity. Various modulation methods can be applied to CHB inverters. CHB inverters can also increase the number of output voltage levels easily by increasing the number of H-bridges. This paper presents a DSTACOM with a proportional integral controller based CHB multilevel inverter for the harmonics and reactive power mitigation of the nonlinear loads. This type of arrangements have been widely used for PQ applications due to increase in the number of voltage levels, low switching losses, low electromagnetic compatibility for hybrid filters and higher order harmonic elimination.

II. DESIGN OF MULTILEVEL BASED DSTACOM

A. Principle of DSTACOM

A D-STATCOM (Distribution Static Compensator), which is schematically depicted in Figure-1, consists of a two-level Voltage Source Converter (VSC), a dc energy storage device, a coupling transformer connected in shunt to the distribution network through a coupling transformer. The VSC converts the dc voltage across the storage device into a set of three-phase ac output voltages. These voltages are in phase and coupled with the ac system through the reactance of the coupling transformer. Suitable adjustment of the phase and magnitude of the D-STATCOM output voltages allows effective control of active and reactive power exchanges between the DSTACOM and the ac system. Such configuration allows the device to absorb or generate controllable active and reactive power.

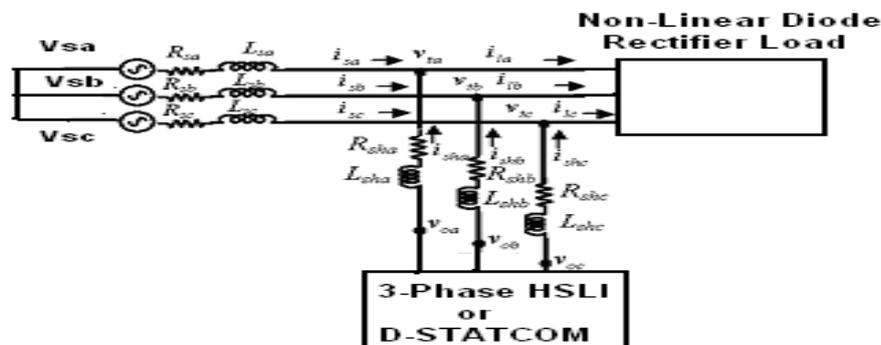


Figure – 1 Schematic Diagram of a DSTACOM

The VSC connected in shunt with the ac system provides a multifunctional topology which can be used for up to three quite distinct purposes:

1. Voltage regulation and compensation of reactive power;
2. Correction of power factor
3. Elimination of current harmonics.

B. Control for Reactive Power Compensation

The aim of the control scheme is to maintain constant voltage magnitude at the point where a sensitive load under system disturbances is connected. The control system only measures the rms voltage at the load point, i.e., no reactive power measurements are required. The VSC switching strategy is based on a sinusoidal PWM technique which offers simplicity and good response. Since custom power is a relatively low-power application, PWM methods offer a more flexible option than the fundamental frequency switching methods favored in FACTS applications. Apart from this, high switching frequencies can be used to improve on the efficiency of the converter, without incurring significant switching losses.

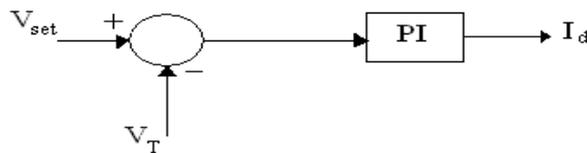


Figure-2 PI control for reactive power compensation

The controller input is an error signal obtained from the reference voltage and the rms terminal voltage measured. Such error is processed by a PI controller; the output is the angle δ , which is provided to the PWM signal generator. It is important to note that in this case, of indirectly controlled converter, there is active and reactive power exchange with the network simultaneously. The PI controller processes the error signal and generates the required angle to drive the error to zero, i.e. the load rms voltage is brought back to the reference voltage.

C. Control for Harmonics Compensation

The Modified Synchronous Frame method is presented in [7]. It is called the instantaneous current component (i_d - i_q) method. This is similar to the Synchronous Reference Frame theory (SRF) method. The transformation angle is now obtained with the voltages of the ac network. The major difference is that, due to voltage harmonics and imbalance, the speed of the reference frame is no longer constant. It varies instantaneously depending of the waveform of the 3-phase voltage system. In this method the compensating currents are obtained from the instantaneous active and reactive current components of the nonlinear load. In the same way, the mains voltages $V(a,b,c)$ and the available currents $i_1(a,b,c)$ in α - β components must be calculated as given by (4), where C is Clarke Transformation Matrix. However, the load current components are derived from a SRF based on the Park transformation, where ' θ ' represents the instantaneous voltage vector angle (5).

Table-1 Switching table of single CHB inverter

Switches Turn ON	Voltage Level
S1,S2	Vdc
S3,S4	-Vdc
S4,D2	0

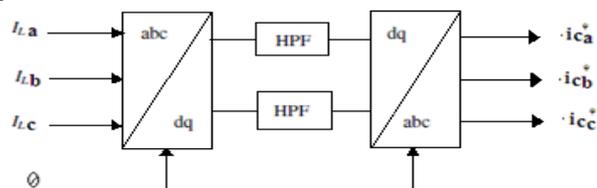


Figure-3 Block diagram of SRF method

D. Cascaded H-Bridge Multilevel Inverter

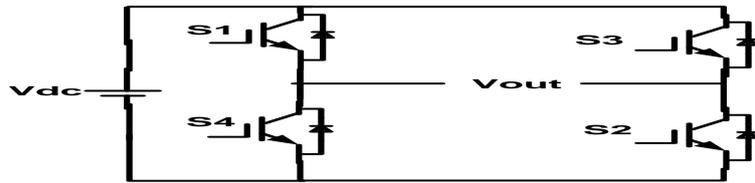


Figure-4 Circuit of the single cascaded H-Bridge Inverter

Fig.4 shows the circuit model of a single CHB inverter configuration. By using single H-Bridge we can get 3 voltage levels. The number of output voltage levels of CHB is given by $2n+1$ and voltage step of each level is given by $V_{dc}/2n$, where n is number of H-bridges connected in cascaded. The switching table is given in Table 1.

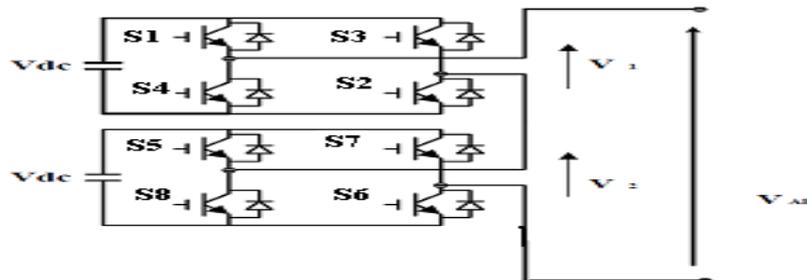


Figure-5 Block diagram of 5-level CHB inverter model

The switching mechanism for 5-level CHB inverter is shown in table-2.

Table 2. Switching table for 5-level CHB Inverter

Switches Turn On	Voltage Level
S1, S2	V_{dc}
S1, S2, S5, S6	$2V_{dc}$
S4, S8, S7, S6	0
S3, S4	$-V_{dc}$
S3, S4, S7, S8	$-2V_{dc}$

E. PWM Techniques for CHB Inverter

The most popular PWM techniques for CHB inverter are 1. Phase Shifted Carrier PWM (PSCPWM), 2. Level Shifted Carrier PWM (LSCPWM).

1. Phase Shifted Carrier PWM (PSCPWM)

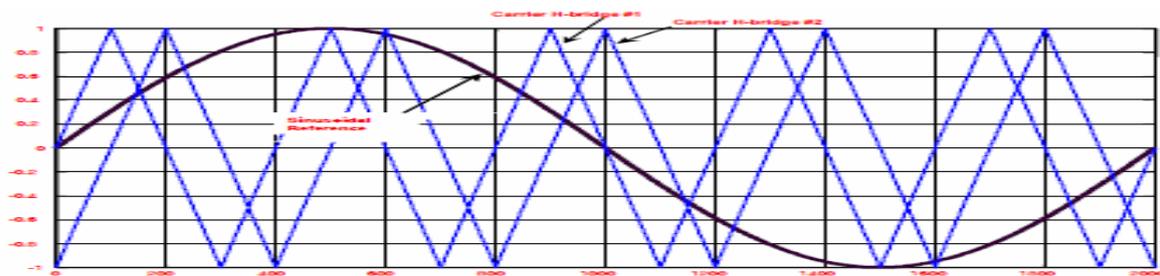


Fig. 6 phase shifted carrier PWM

Fig6 shows the Phase shifted carrier pulse width modulation. Each cell is modulated independently using sinusoidal unipolar pulse width modulation and bipolar pulse width modulation respectively, providing an even power distribution among the cells. A carrier phase shift of $180^\circ/m$ (No. of levels)

for cascaded inverter is introduced across the cells to generate the stepped multilevel output waveform with lower distortion.

2. Level Shifted Carrier PWM (LSCPWM)

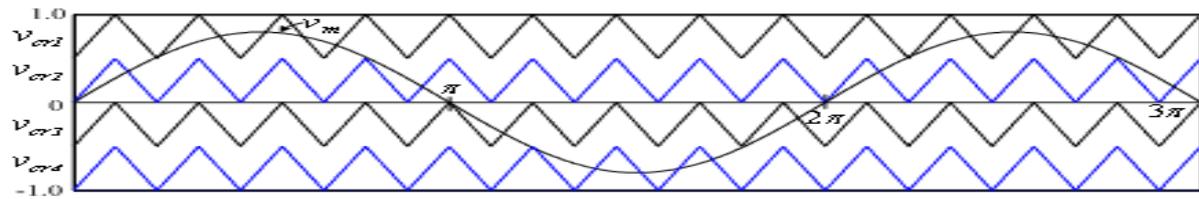


Fig.7 Level shifted carrier PWM

Fig.7 shows the Level shifted carrier pulse width modulation. Each cell is modulated independently using sinusoidal unipolar pulse width modulation and bipolar pulse width modulation respectively, providing an even power distribution among the cells. A carrier Level shift by $1/m$ (No. of levels) for cascaded inverter is introduced across the cells to generate the stepped multilevel output waveform with lower distortion.

III. MATLAB/SIMULINK MODELING AND SIMULATION RESULTS

Here Matlab/Simulink model is developed for two cases. In case one DSATCOM with Linear load and in case two DSTATCOM with nonlinear load are simulated.

A. Case one

Fig8 shows the Matlab/Simulink power circuit model of DSTATCOM. It consists of five blocks named as source block, non linear load block, control block, APF block and measurements block.

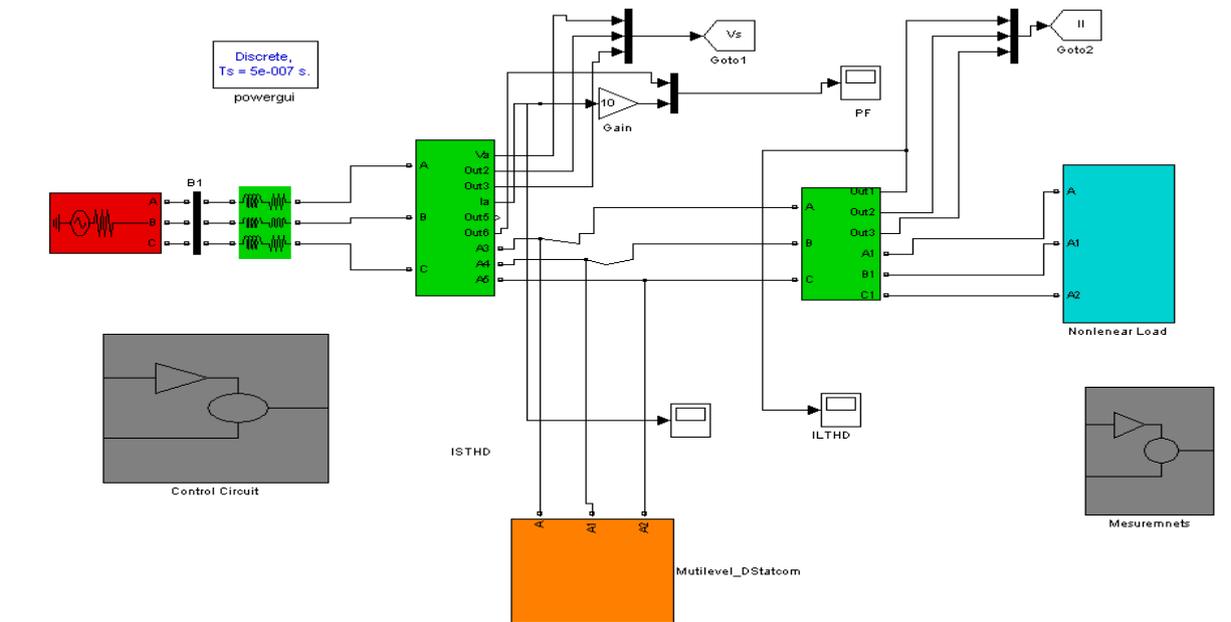


Fig. 8 Matlab/Simulink power circuit model of DSTATCOM

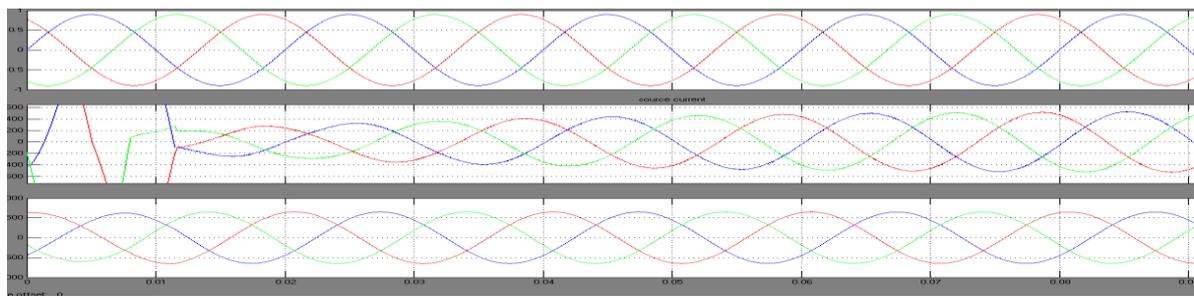


Fig. 9 Source voltage, current and load current with DSTATCOM

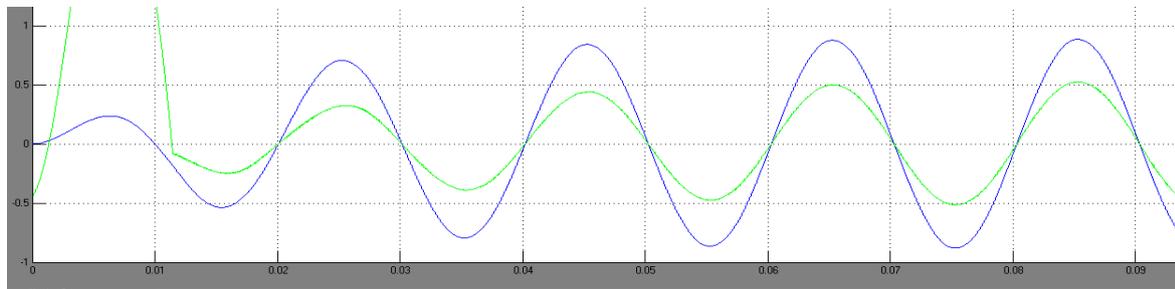


Fig.10 Phase-A source voltage and current

Fig.10 shows the phase-A source voltage and current, even though the load is non linear RL load the source power factor is unity.

B. Case two

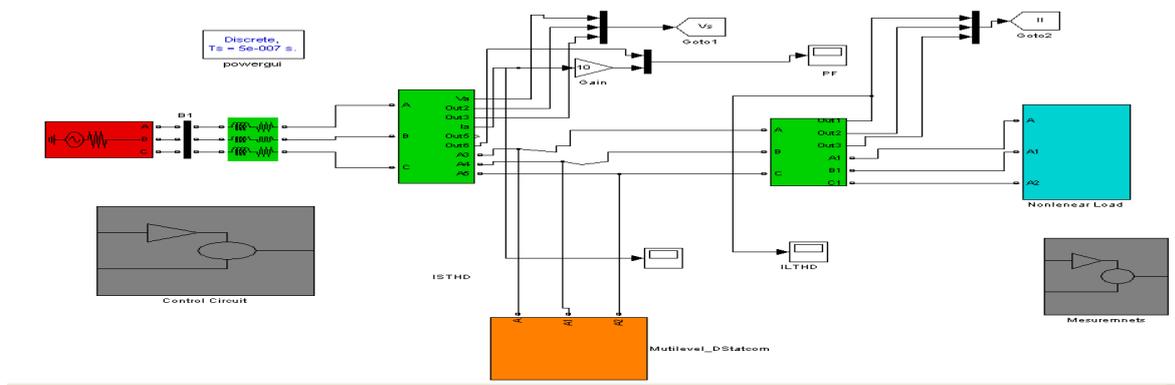


Fig.11 Matlab/Simulink power circuit model of DSTATCOM

Fig. 11 shows the phase-A voltage of five level output of phase shifted carrier PWM inverter.

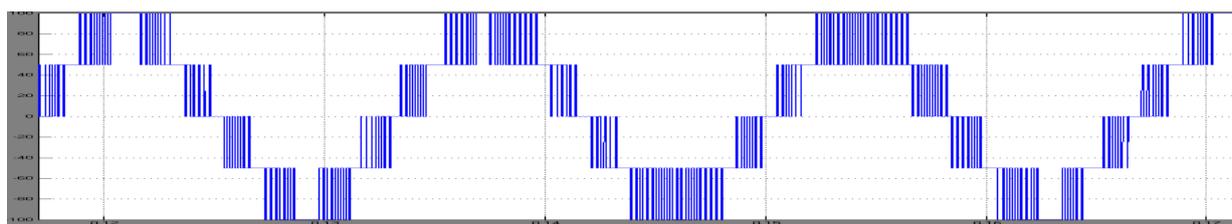


Fig. 12 five level PSCPWM output

Fig. 13 shows the three phase source voltages, three phase source currents and load currents respectively without DSTATCOM. It is clear that without DSTATCOM load current and source currents are same.

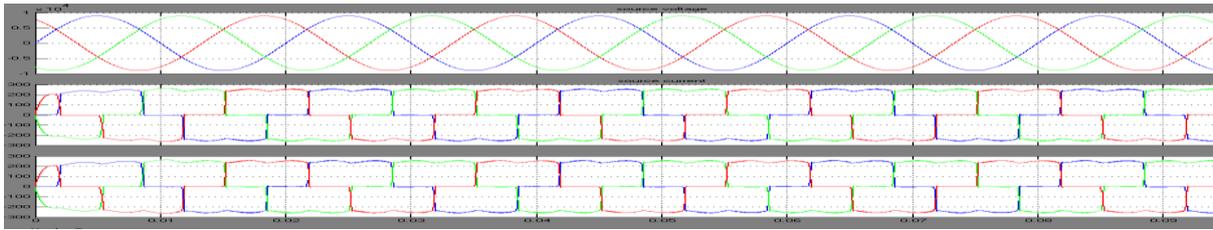


Fig. 13 Source voltage, current and load current without DSTATCOM

Fig. 14 shows the three phase source voltages, three phase source currents and load currents respectively with DSTATCOM. It is clear that with DSTATCOM even though load current is non sinusoidal source currents are sinusoidal.

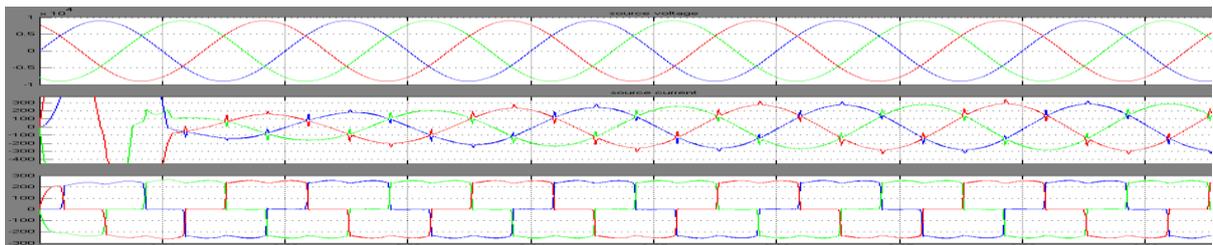


Fig. 14 Source voltage, current and load current with DSTATCOM

Fig. 15 shows the DC bus voltage. The DC bus voltage is regulated to 11kv by using PI regulator.

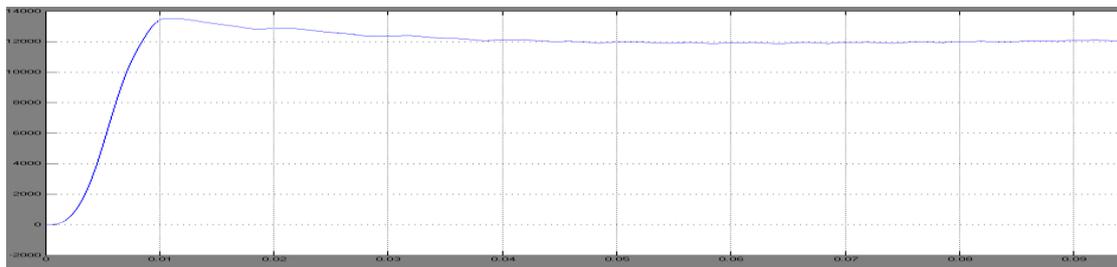


Fig. 15 DC Bus Voltage

Fig. 16 shows the phase-A source voltage and current, even though the load is non linear RL load the source power factor is unity.

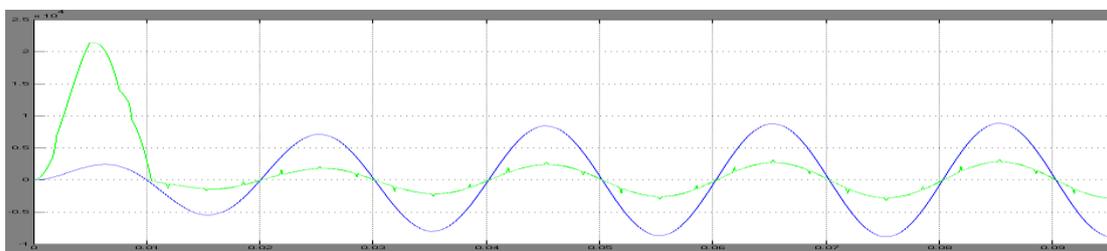


Fig. 16 Phase-A source voltage and current

Fig. 17 shows the harmonic spectrum of Phase –A Source current without DSTATCOM. The THD of source current without DSTACOM is 36.89%.

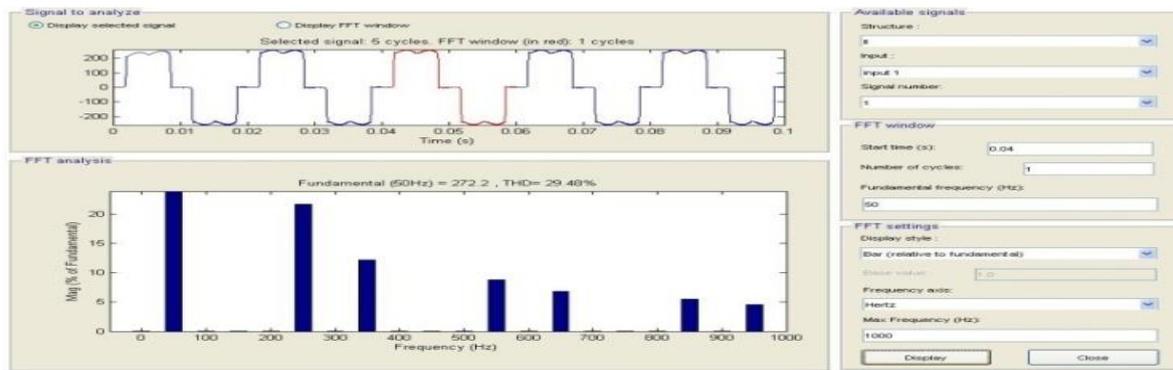


Fig. 17 Harmonic spectrum of Phase-A Source current without DSTATCOM

Fig. 18 shows the harmonic spectrum of Phase –A Source current with DSTATCOM. The THD of source current without DSTACOM is 5.05%

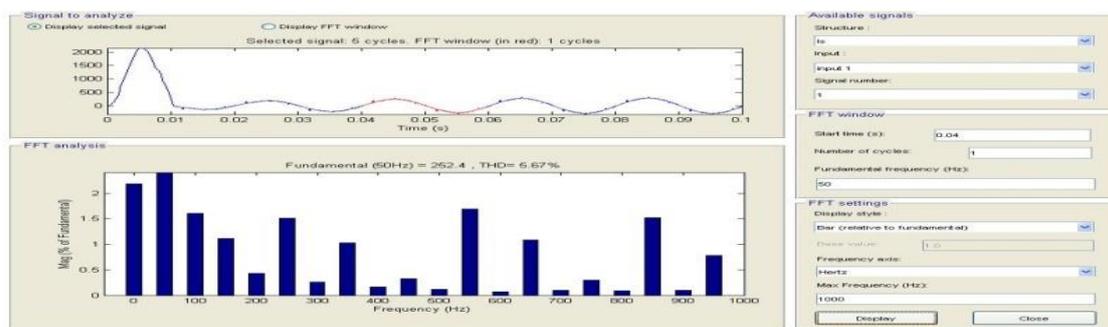


Fig. 18 Harmonic spectrum of Phase-A Source current with DSTATCOM

IV. CONCLUSION

This paper studied a five level inverter used in a DSTATCOM in PS and has been successfully demonstrated in MatLab/Simulink. The benefits of five level inverter has low harmonics distortion, reduced number of switches to achieve the seven- level inverter output over the cascaded seven level inverter and reduced switching losses. A DSTATCOM with five level CHB inverter is investigated. Mathematical model for single H-Bridge inverter is developed which can be extended to multi H-Bridge. The source voltage , load voltage , source current, load current, power factor simulation results under non-linear loads are presented. Finally Matlab/Simulink based model is developed and simulation results are presented for both linear and non linear loads

REFERENCES

- [1]. K.A Corzine, and Y.L Familant, “A New Cascaded Multi-level H-Bridge Drive,” IEEE Trans. Power.Electron., vol.17, no.1, pp.125-131. Jan 2002.
- [2]. J.S.Lai, and F.Z.Peng “Multilevel converters – A new bread of converters, ”IEEE Trans. Ind.Appli., vol.32, no.3, pp.509-517. May/ Jun. 1996.
- [3]. T.A.Maynard, M.Fadel and N.Aouda, “Modelling of multilevel converter,” IEEE Trans. Ind.Electron., vol.44, pp.356-364. Jun.1997.
- [4]. P.Bhagwat, and V.R.Stefanovic, “Generalized structure of a multilevel PWM Inverter,” IEEE Trans. Ind. Appln, Vol.1A-19, no.6, pp.1057-1069, Nov./Dec..1983.
- [5]. J.Rodriguez, Jih-sheng Lai, and F Zheng peng, “Multilevel Inverters; A Survey of Topologies, Controls, and Applications,” IEEE Trans. Ind. Electron., vol.49 , no4., pp.724-738. Aug.2002.
- [6]. Roozbeh Naderi, and Abdolreza rahmati, “Phase-shifted carrier PWM technique for general cascaded inverters,” IEEE Trans. Power.Electron., vol.23, no.3, pp.1257-1269. May.2008.
- [7]. Bhim Singh, Kamal AlHaddad & Ambrish Chandra, 1999, A Review of Active Filter for Power Quality Improvements, IEEE Trans on Industrial Electronics, 46(5), pp.960970

- [8]. Mauricio Angulo, Pablo Lezana, Samir Kouro, Jos'e Rodr'iguez and Bin Wu, "Level-shifted PWM for Cascaded Multilevel Inverters with Even Power Distribution" IEEE Power Electronics specialist conference, 17-21 june 2007, pp.2373-2378.
- [9]. P. McGrath and D. G. Holmes, "Multicarrier PWM strategies formultilevel inverters," IEEE Trans. Ind. Electron., vol. 49, no. 4, pp. 858–867, August 2002.
- [10]. M. Meinhardt and G. Cramer, "Past, present and future of grid-connected photovoltaic- and hybrid-power-systems," in Proc. IEEE-PES Summer Meeting, Jul. 2000, vol. 2, pp. 1283–1288.
- [11]. S. Kouro, J. Rebolledo, and J. Rodriguez, "Reduced switching-frequency modulation algorithm for high-power multilevel inverters," IEEE Trans.Ind. Electron, vol. 54, no. 5, pp. 2894–2901, Oct. 2007.
- [12]. S. J. Park, F. S. Kang, M. H. Lee, and C. U. Kim, "A new single-phase five level PWM inverter employing a deadbeat control scheme," IEEE Trans. Power Electron., vol. 18, no. 18, pp. 831–843, May 2003.
- [13]. L. M. Tolbert and T. G. Habetler, "Novel multilevel inverter carrier-based PWM method," IEEE Trans. Ind. Appl., vol. 35, no. 5, pp. 1098–1107, Sep./Oct. 1999.
- [14]. Y. Liu, H. Hong, and A. Q. Huang, "Real-time calculation of switching angles minimizing THD for multilevel inverters with step modulation," IEEE Trans. Ind. Electron., vol. 56, no. 2, pp. 285–293, Feb. 2009.
- [15]. N. S. Choi, J. G. Cho, and G. H. Cho, "A general circuit topology of multilevel inverter," in Proc. IEEE 22th Annu. PESC, Jun. 24–27, 1991, pp. 96–103.
- [16]. Holmes, D. G. and Lipo, T. A., Pulse width modulation for power converters: principles and practice, IEEE.
- [17]. T.H.Barton, "Pulse Width Modulation Waveforms – The Bessel Approximatilon", IEEE-IAS Conference Record,

AUTHORS

Arun Kumar Rath received his M. Tech Degree in Power Electronics and Drives from GIET, Gunupur under BPUT UG from BPUT. A life time member of ISTE and also a life time member of SESI & IAENG. He working as an Asst. professor in EEE Department at Gandhi institute of engineering & Technology. He is having overall more than 9 years experiences in Industrial and teaching fields. His interest areas are Power system engineering and Power Electronics & smart grid technologies.



Srikant Misra received his M. Tech Degree in Power Electronics and Drives from GIET, Gunupur under BPUT UG from BPUT. A life time member of ISTE and also a life time member of SESI. He working as an Asst. professor in EEE Department at Gandhi institute of engineering & Technology. He is having overall more than 7 years experiences in Industrial and teaching fields. His interest areas are Renewable power system and Power Electronics.



Ch. Venkateswara Rao received his M.Tech degree from JNTUK, kakinada and U.G from IE (India), Kolkata) in the year 1993. A life member in ISTE and IAENG. This Author won first prize in Energy conservations Award for the year 2009. He is currently working as a professor in the department of EEE in Gandhi Institute. of Engineering and Technology, Gunupur, Odisha He guided many.UG & PG Projects. He is having overall Industrial &Teaching experience of 18 years. His major Research interests are Energy Conservation and Smart Grid technologies.

