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HIGH PERFORMANCE CASCADED MULTILEVEL INVERTER FED BRUSHLESS DC MOTOR DRIVE

A. Purna Chandra Rao[1], Y.P. Obulesh[2], Ch. Sai Babu[3]
[1]Department of EEE, Prasad V. Potluri Siddhartha Institute of Technology, Andhra Pradesh
alapati.purna@yahoo.com
[2]Department of EEE , Lakireddy Bali Reddy College of Engineering, Andhra Pradesh
ypobulesh@yahoo.co.in
[3]Department of EEE, J.N.T University Kakinada, Kakinada,Andhra Pradesh
chs_eee@yahoo.co.in

ABSTRACT

In this paper, a modular three-phase multilevel inverter topology for brushless dc motor drive has been proposed. Unlike conventional H Bridge inverter, this topology is based on power cells connected in cascade, each power cell is consisting of two inverter legs in series. In this new topology input voltage is Vdc/2 ,when both the switches in same leg conducts simultaneously means the short circuit of power source, at this point half power is dissipated through the switch and the severity of explosion of power cell is reduced to half and it enhances the reliability of the system and cost effectual. A detailed analysis of the proposed structure with five levels are carried out using pulse width-modulation phase-shifted multicarrier modulation. Finally five level Cascaded multilevel inverter fed Brushless dc motor drive is implemented in Matlab/ Simulink and simulation results are presented.

KEYWORDS- *Cascade systems, inverters, multilevel systems, pulse width modulation (PWM). Medium-voltage drives, multilevel converter topologies.*

I. INTRODUCTION

In a regular Brush Less DC motor (BLDC) drive, the motor in general fed with Pulse Width-Modulated (PWM) voltages which cause steep voltage wave fronts (*dv/dt*) to materialize across the motor terminals. This may possibly escort the motor insulation stoppage. In addition, motor damages are reported due to the high-voltage change rates (*dv/dt*) which produces common-mode voltages athwart the motor windings. Elevated frequency switching increases the gravity of this drawback due to the increased number of times. In each cycle this common-mode voltage is functional [1]–[3]. For variable-speed medium-voltage drives this is a piece of big concern where the voltage levels are incredibly far above the ground. The expected problem can be resolved by applying variable voltage with low *dv/dt* i.e., making the use of multilevel inverter.

Multilevel inverters [4], [5] have been attracting wide industrialized significance they are taken as an impressed alternative in order to reduce switch stress. An output waveform with multiple voltage levels is the main characteristic of these converters. By escalating the number of procedures of the motor voltage as in multicell technologies [6], [7], the reduced gravity problem is occurred. Besides that, the multilevel inverters can efficiently work at lower switching frequencies when compared to conventional PWM inverters [8]. In recent decades, a widespread array of multilevel structures has appeared [9]–[13], for instance, the cascaded H-bridge (CHB), neutral point clamped, and flying capacitor. Similar voltage profiles can be acquired by means of higher order neutral-point-clamped (NPC) multilevel inverters [15], [16] or by cascading a number of two-level inverters. Nevertheless, the multilevel NPC inverters undergo dc-bus imbalance [17], device underutilization problems and imbalanced ratings of the clamped diodes and so forth., which are not very severe harms for inverters with three levels or lesser. The capacitor voltage imbalance for a five-level one is presented in which put forward the necessitate of extra hardware in the form of dc choppers or a back-to-back connection of multilevel converters. The CHB multilevel inverter is a topology of all the rage and

has found prevalent applications in industry, in high- power medium-voltage drives as well as reactive power compensation. It is self-possessed with various units of single- phase H-bridge power cells, using two inverter legs in parallel motorized by isolated dc supplies. The inverter dc bus voltage is regularly fixed, whereas its ac output voltage could be attuned by different modulation schemes. The dc supplies are normally obtained by multi pulse diode rectifier to attain low line current harmonics distortion along with high input power factor. The H-bridge cells are generally allied in cascade on relevant ac side to achieve medium-voltage operation and low harmonic deformation. In practice, the amount of power cells in a CHB inverter is chiefly resolute by its operating voltage and manufacturing outlay. The exploit of one and the same power cells results in modular structure, which is an efficient way for cost reduction. Cascaded multilevel inverters have been build up to exploit unequal dc bus voltages or a single dc source, showing the likelihood of various achievements for existing topology. The cascaded H-bridge topology suffers from the downside of the procedure of huge dc-bus capacitors and complex input transformers for isolated dc bus for each module. These drawbacks are focused in the planned topology. In addition, the power circuit is modular in structure, and consequently, the number of modules to be associated in series depends on the power of the drive. The key drawback of CHB is that if two switches in same leg are turned on creates a short circuit of power cell and get damaged to overcome this problem we need to replace all the power cell which is pricey and time devastate.

In this proposed topology, power cells linked in cascade using two inverter legs in series, as an alternative of two parallel inverter legs, set up in CHB power cells, conservatively. In this proposed topology input voltage is Vdc/2 and in condition any module goes amiss, and the topology can maneuver with shortened output voltage and consequently reduced power. So that severity of explosion is reduced to half and results in increase of the reliability of the system and cost effectual. A detailed analysis of the proposed structure with five levels are carried out using pulse width-modulation phase-shifted multicarrier modulation. Finally five level Cascaded multilevel inverter fed Brushless dc motor drive is implemented in Matlab / Simulink and simulation results are presented for verification and validation of the proposed work.

II. PROPOSED TOPOLOGY FOR BLDC MOTOR DRIVE

The proposed three-phase multilevel inverter is fed BLDC motor shown in Fig. 1. This inverter is unruffled with (3LLv−3) switches and (3LLv−3)/2 isolated dc voltage sources, where LLv is the add up to voltage levels of the line-to-line output voltage. The load can be connected in delta or wye. A basic inverter leg with two switches, functioning in an identical way, is revealed in Fig. 2(a). Each power cell is a marshal of two inverter legs with the connections defined in Fig. 2(b). Voltage VC (t) is shown in Fig. 2(b) is collected of three voltage levels: Vdc , 0, and −Vdc . When switches $S_R(n-1)$ and S_Rn conduct, the output voltage in the power cell is VC (t) = Vdc . Equally, with $S_R(n-1)^1$ and S_Rn^1 switched on,VC(t) = −Vdc. To obtain the level zero, the switches $S_R(n-1)$ and S_Rn^1 or $S_R(n-1)^1$ and S_Rn are supposed to be turn on. As a consequence, by concerning the power cells in cascade as shown in Fig. 3, with a certain phase shift in the switch command flanked by two power cells in the identical phase, the number of voltage levels from phase-to-neutral voltage (Pnv) can be increased subjectively.

The utmost figures of voltage levels of the line-to-line output voltage Vab(t) and phase-to-neutral voltage Van(t) are respectively represented by

$$LLv=4Npc + 1 \quad (1)$$

$$Pnv =2Npc + 1 \quad (2)$$

Where Npc is the number of power cells per phase. By edifice, in this topology, the number of voltage levels is odd always.

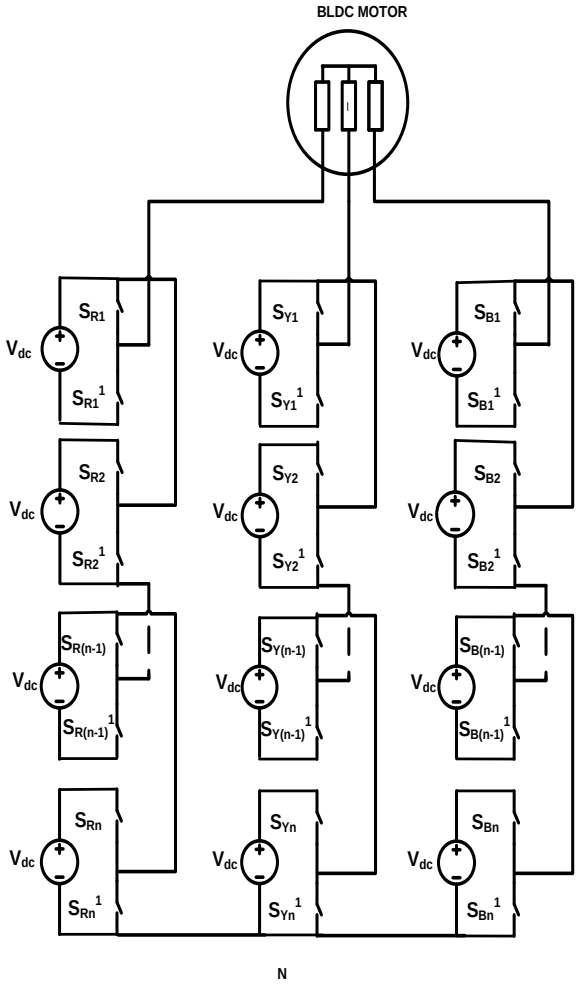

Fig.1. Proposed Multilevel inverter fed BLDC Drive

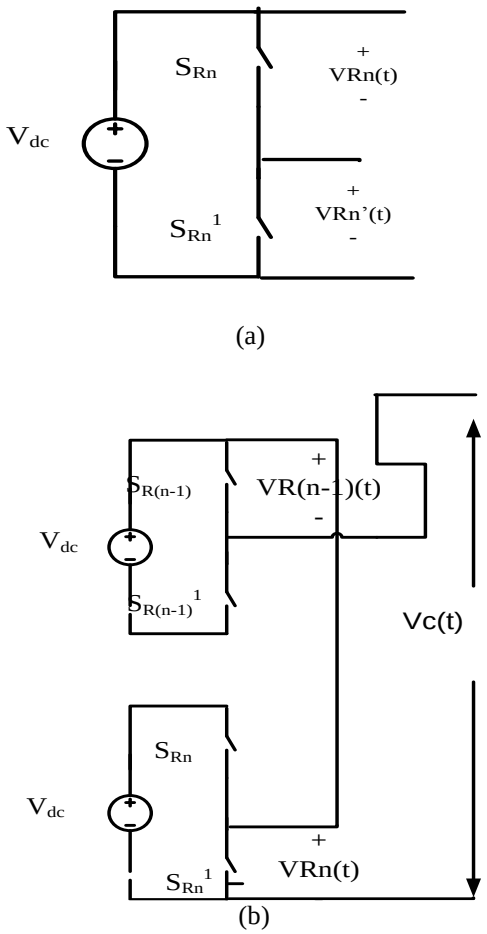

Fig. 2. (a) Isolated dc voltage source connected to inverter leg.
(b) Power cell using two inverter legs connected in series.

III. IMPLEMENTATION OF THE PROPOSED MULTILEVEL INVERTER TOPOLGY WITH PHASE SHIFTED CARRIER PWM (PSCPWM) MODULATION STRATEGY

Fig. 4 shows, a Pulse Width-Modulation (PWM) technique. Every bit of the triangular carriers have the similar occurrence in frequency and the identical peak to peak amplitude and phase shift between two adjoining carrier waves to enhance harmonic annulment.
A phase shift classified by

$$\frac{(K-1)\pi}{Nc} \quad K = 1,2,3,4 \dots \dots 2Nc$$

designed for an inverter with two power cells in cascade, it is necessary to occupy four triangular carriers with phase shifts of 0, π/2, π, and 3π/2.
Switch-gate signals for one phase are shown in Fig. 4, the other two phases are shifted by ±120◦. To achieve the switch-gate signals, a similarity between the triangular carriers and the modulator is approved shown in Fig. 4. The ensuing signal would be lofty when the instantaneous values of the sinusoidal wave surpass the triangular carrier; or else, it would be lowered. These high-frequency pulses are sent to the switches of the circuit in Fig. 1, with four inverter legs in cascade.

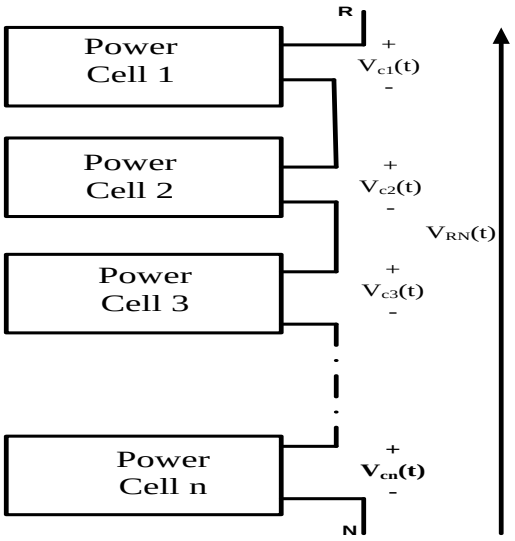

Fig.3. Cascade Per-phase diagram of power cells **Fig. 4** Simulated waveform of the proposed multilevel inverter

The carrier waveforms engaged in particular modulation technique are habitually triangular or saw tooth. In this paper, the triangular unipolar format was used for the reason that it reduces the harmonic content when evaluated with the saw tooth carrier. Triangular carriers have a fixed scale, on the whole, so the fundamental magnitude control of the output voltage is attained by altering the sinusoidal modulator amplitude. This results in alteration of the pulse widths shifting the output voltage amplitude. In Fig. 5, the modulation schematic is given. The phase-shift modulation portrayed here is comparable to the one used in CHB multilevel inverters. A CHB multilevel inverter with np voltage levels entails (np − 1) triangular carriers. In the phase-shifted multicarrier modulation, all the triangular carriers embrace the identical frequency and the same peak-to-peak amplitude, in the company of a phase shift between any two neighboring carrier waves. Nevertheless, the phase shift involving two parallel inverter legs of each power cell ought to be 180◦. All comparators share the same modulator waveform, and each unipolar triangular carrier has an unwavering shift. The proposed CHHB uses less number of switches to fabricate supplementary voltage levels. This will shrink Gate Drivers and protection circuit requirement accordingly it diminish cost and intricacy of the circuit.

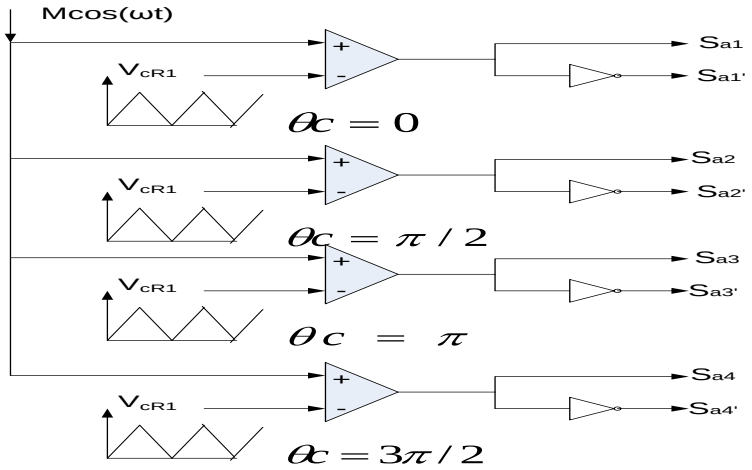

Fig.5. Modulation schematic

IV. SIMULATION RESULTS

A. Proposed five level multilevel inverter fed BLDC drive

The proposed cascade half bridge cell multilevel inverter fed BLDC motor with phase shifted PWM modulation technique has been developed using Matlab / Simulink software and results are presented. Fig. 6 Shows the Matlab / Simulink model of three phase cascaded half bridge inverter fed BLDC motor drive and Fig. 7 shows the inside view of one phase leg. Fig 8 shows the phase voltage of converter output voltage and Fig 9. Shows the line to line output voltage of the proposed converter .Fig.10 and fig 11 shows the speed response and torque developed by the proposed converter fed BLDC motor.

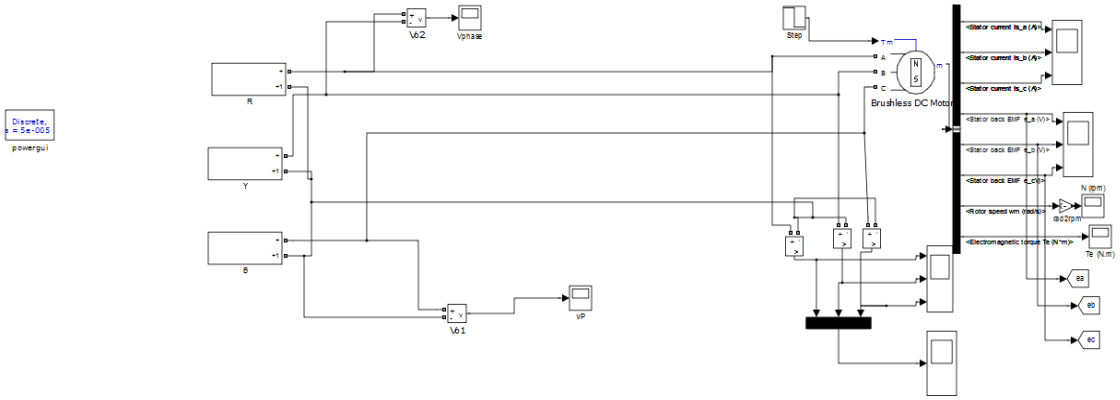

Fig. 6. Simulink model of Cascaded Half Bridge Cells fed BLDC motor

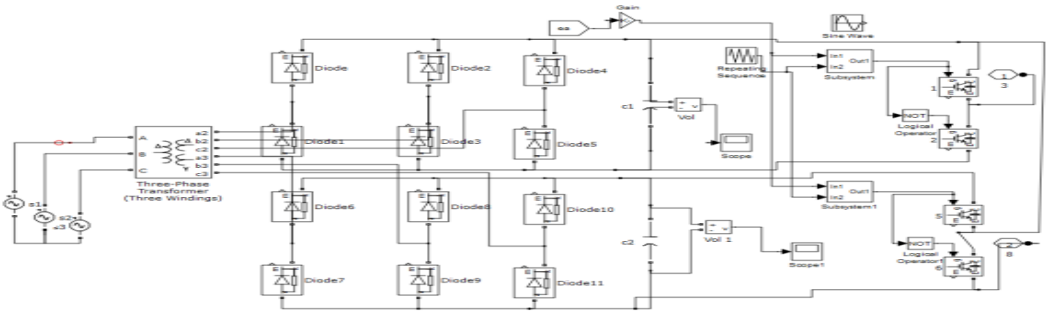

Fig.7. Simulink model R phase cascade half bridge cell

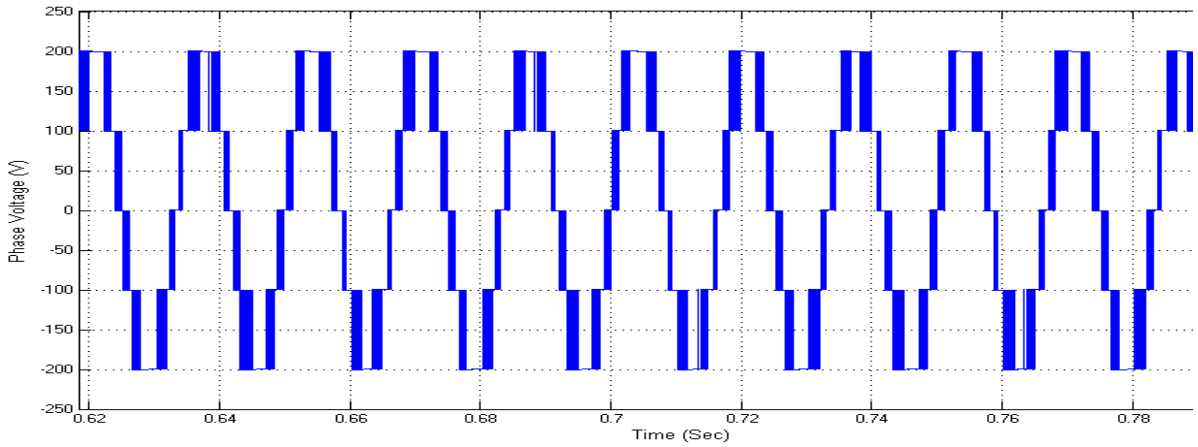

Fig.8. MLI Phase voltage

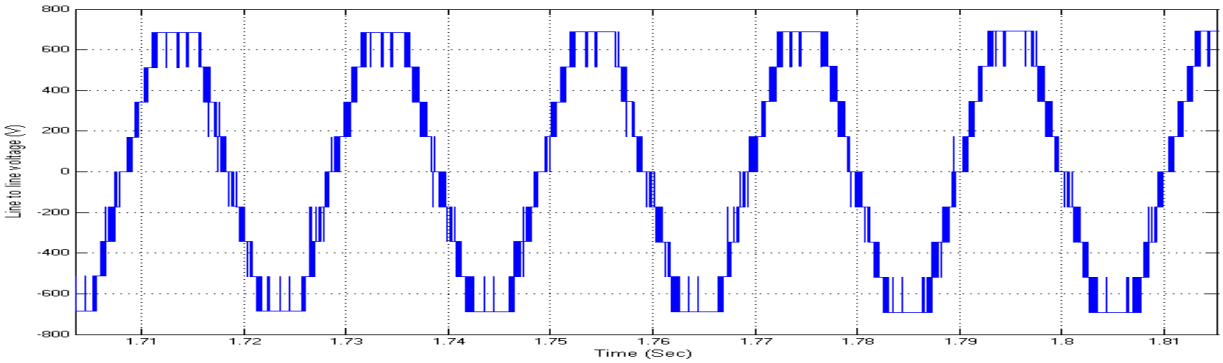

Fig. 9. Output Nine level Line to line voltage

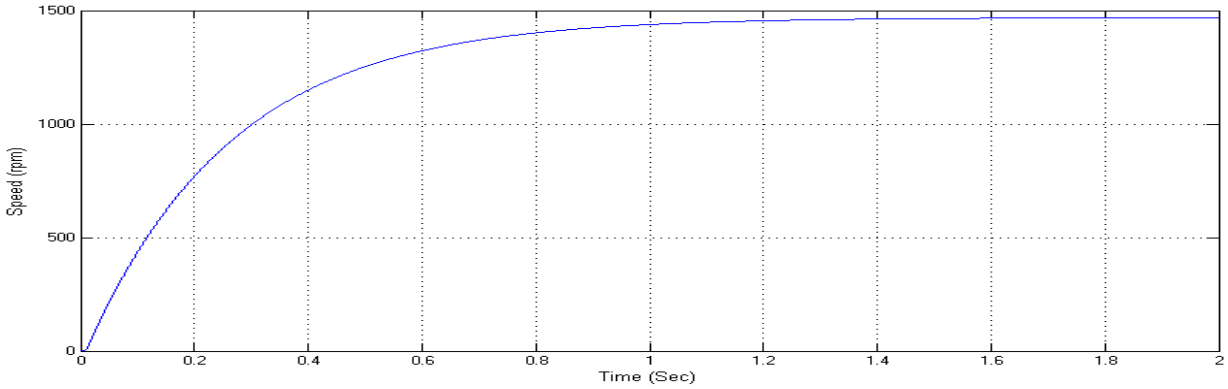

Fig. 10 Output Speed in rpm

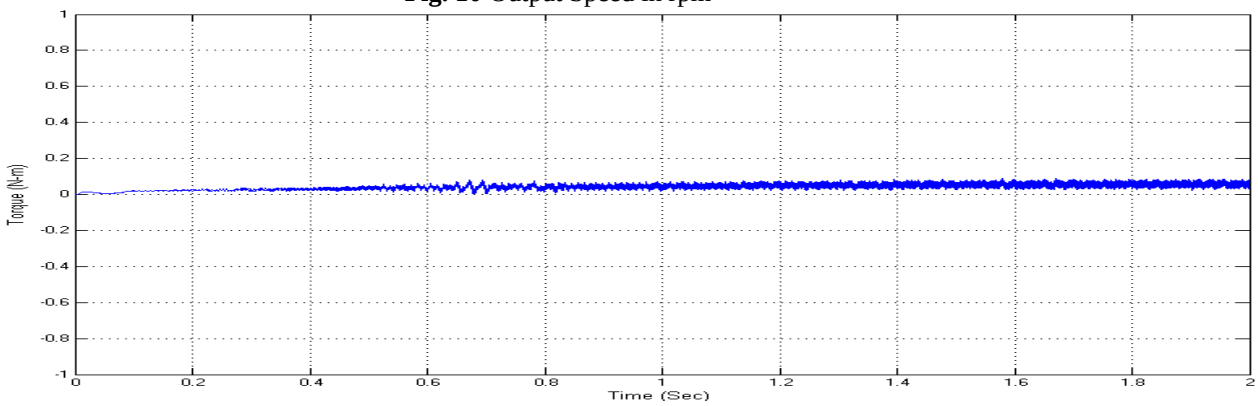

Fig. 11 Output Torque in N-m

B. Phase Shifted Carrier PWM Five Level CHB MLI fed BLDC motor

Fig.12 and Fig.13 shows output speed and the generated torque of the 5-level CHB inverter fed BLDC motor with phase shifted PWM modulation technique. The behavior of the generated electromagnetic torque is also of vital importance. The stator back-emf for each phase is shown in Fig.14. Fig.15 shows the five levels of three phase output voltage of the CHB phase shifted PWM Inverter.

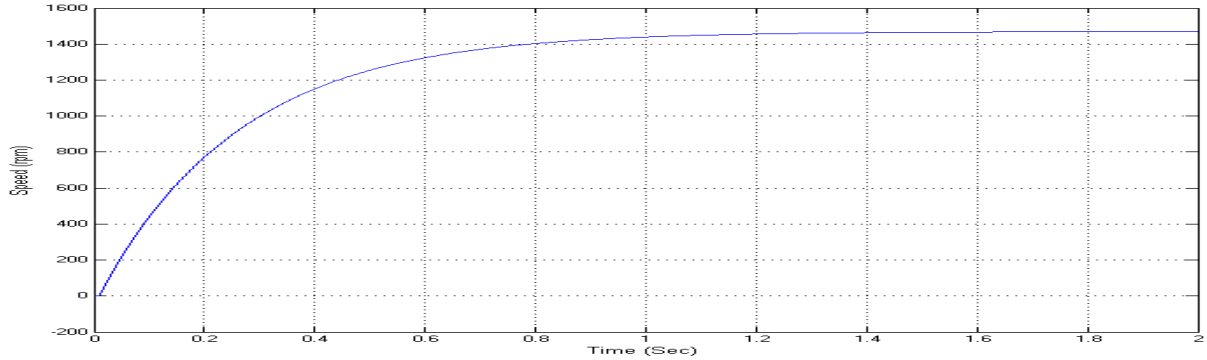

Fig.12. Output Speed of 5-level CHB inverter fed BLDC motor

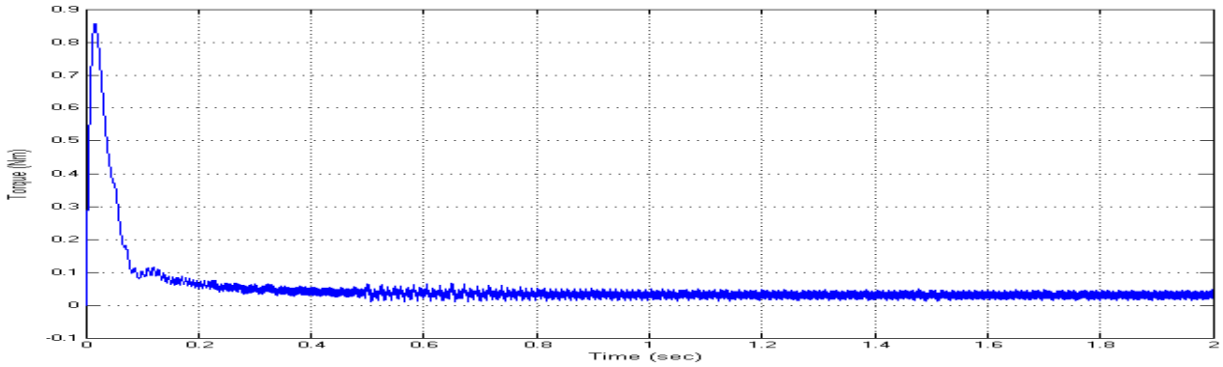

Fig.13. Electro Magnetic Torque of 5-level CHB inverter fed BLDC motor

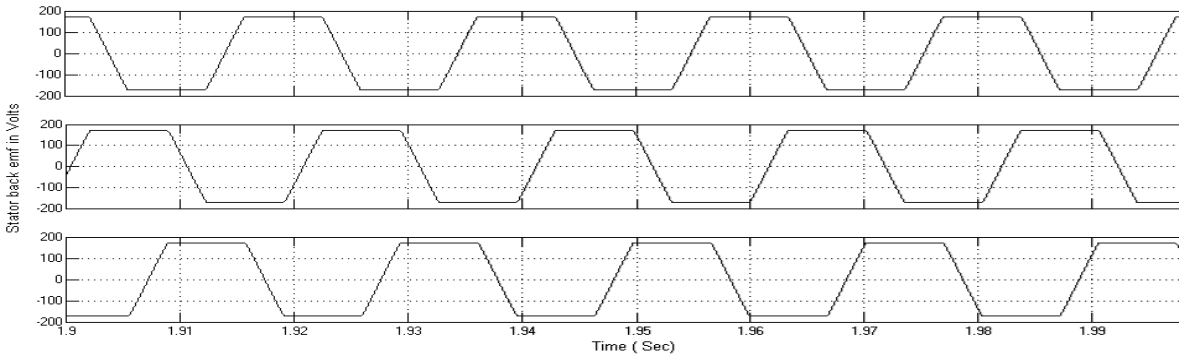

Fig.14. Three Phase Stator Back-EMFs

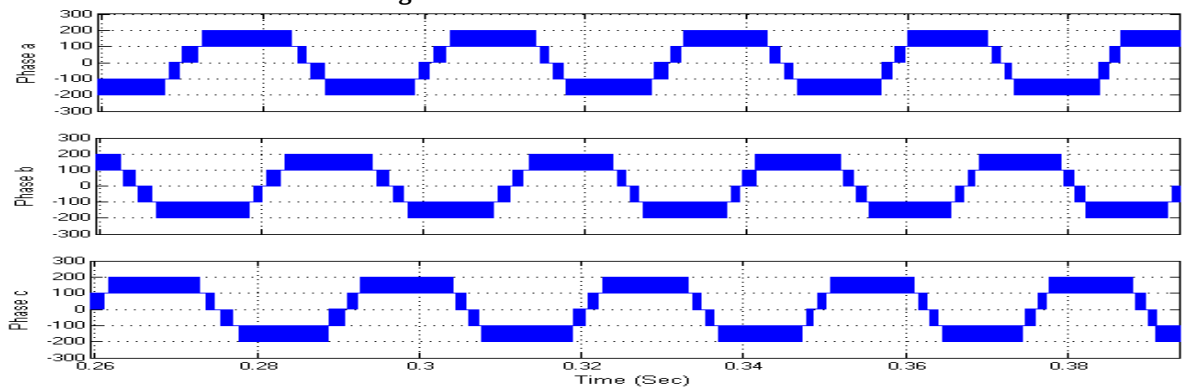

Fig.15. Five Level Output Voltages with phase shifted PWM modulation technique

V. COMPARISON BETWEEN THE PRO POSED INVERTER AND CHB MULTILEVEL INVERTER

The foremost disparity among the proposed topology and a CHB inverter is the manner how the inverter legs are associated. These two converters have the same number of switches on each power module, by this means, the voltage levels generated in the terminals of each power cell are the equivalent. In consequence the numbers of voltage levels of the phase-to-neutral voltage (VAN) and line- to-line output voltage (VAB) will result in equal, as described in Table I. Each power module in the proposed topology employs double the number of isolated dc voltage sources, with the power reduced half. The PWM phase-shifted multicarrier modulation technique drawn in the proposed topology is comparable to that used in CHB multilevel inverters.

TABLE 1 : Comparison Between Cascade H Bridge Multilevel Inverter And The Proposed Topology

	CHB Multilevel inverter	**Proposed Topology**
Phase to neutral voltage levels	P_{nv}	P_{nv}
Line to line voltage levels	$(2P_{nv}-1)$	$(2P_{nv}-1)$
No. of switches per phase	$2(P_{nv}-1)$	$2(P_{nv}-1)$
No.of power module per phase	$(P_{nv}-1)/2$	$(P_{nv}-1)/2$
Output voltage THD	same	same
No. of isolated DC source per phase	$(P_{nv}-1)/2$	$(P_{nv}-1)$
Modulation strategy	same	same
Power of each isolated Dc source	$2P/3(P_{nv}-1)$	$P/3(P_{nv}-1)$

VI. CONCLUSION

The performance of a proposed three-phase multilevel inverter has been investigated and found quite satisfactory. In this proposed topology input voltage is Vdc/2 short circuit of same leg means that half of power fritter away from it and is easy to reinstate that leg which is cost effective and it will also amplify the reliability is the windfall of this topology. An comparison is made between the proposed topology and the CHB multilevel inverter was also presented, showing parallel uniqueness. Matlab/Simulink model is developed and simulation results are presented.

REFERENCES

[1] L. M. Tolbert, F. Z. Peng, and T. G. Habetler, "Multilevel converters for large electric drives," *IEEE Trans. Ind. Appl.*, vol. 35, no. 1, pp. 36–44, Jan./Feb. 1999.
[2] F. Wang, "Motor shaft voltages and bearing currents and their reduc- tion in multilevel medium-voltage PWM voltage-source-inverter drive applications," *IEEE Trans. Ind. Appl.*, vol. 36, no. 5, pp. 1336–1341, Sep./Oct. 2000.
[3] A. Muetze and A. Binder, "Calculation of circulating bearing currents in machines of inverter-based drive systems," *IEEE Trans. Ind. Electron.*, vol. 54, no. 2, pp. 932–938, Apr. 2007.
[4] J. Lai and F. Peng, "Multilevel converters—A new breed of power converters," *IEEE Trans. Ind. Appl.*, vol. 32, no. 3, pp. 509–517, May/Jun. 1996.
[5] C. Hochgraf, R. Lasseter, D. Divan, and T. A. Lipo, "Comparison of multilevel inverters for static VAr compensation," in *Proc. IEEE Ind. Appl. Soc. Annu. Meeting*, 1994, pp. 921–928
[6] P. W. Hammond, "A new approach to enhanced power quality for medium voltage drives," *IEEE Trans. Ind. Appl.*, vol. 33, no. 1, pp. 202–208,Jan./Feb. 1997.
[7] R. Teodorescu, F. Blaabjerg, J. K. Pederson, E. Cengelci, and P. N. Enjeti, "Multilevel inverter by cascading industrial VSI," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 832–838, Aug. 2002.
[8] J. Rodriguez, J. S. Lai, and F. Z. Peng, "Multilevel inverters: A survey of topologies, control and applications," *IEEE Trans. Power Electron.*, vol. 49, no. 4, pp. 724–738, Aug. 2002.
[9] M. Glinka and R. Marquardt, "A new ac/ac multilevel converter family," *IEEE Trans. Ind. Electron.*, vol. 52, no. 3, pp. 662–669, Jun. 2005

[10] J. Rodriguez, S. Bernet, B. Wu, J. O. Pontt, and S. Kouro, "Multi- level voltage-source-converter topologies for industrial medium-voltage drives," *IEEE Trans. Ind. Electron.*, vol. 54, no. 6, pp. 2930–2945, Dec. 2007.

[11] B. Lin and H. Lu, "New multilevel rectifier based on series connection of H-bridge cell," *Proc. Inst. Elect. Eng.—Electron. Power Appl.*, vol. 147, no. 4, pp. 304–312, Jul. 2000.

[12] S. B. Monge, J. Rocabert, P. Rodriguez, S. Alepuz, and J. Bordonau, "Multilevel diode-clamped converter for photovoltaic generators with independent voltage control of each solar array," *IEEE Trans. Ind. Electron.*, vol. 55, no. 7, pp. 2713–2723, Jul. 2008.

[13] J. I. Leon, S. Vazquez, A. J. Watson, L. G. Franquelo, P. W. Wheeler, and J. M. Carrasco, "Feed-forward space vector modulation for single-phase multilevel cascaded converters with any DC voltage ratio," *IEEE Trans. Ind. Electron.*, vol. 56, no. 2, pp. 315–325, Feb. 2009.

[14] T. A. Meynard and H. Foch, "Multi-level conversion: High voltage chop- pers and voltage-source inverters," in *Proc. 23rd IEEE Power Electron. Spec. Conf.*, Jun. 29–Jul. 3, 1992, vol. 1, pp. 397–403.

[15] A. Nabae, I. Takahashi, and H. Akagi, "A new neutral point clamped inverter," *IEEE Trans. Ind. Appl.*, vol. 17, no. 5, pp. 518–523, Sep./Oct. 1981.

[16] J.-S. Lai and F. Z. Peng, "Multilevel converters—A new breed Of power converters," *IEEE Trans. Ind. Appl.*, vol. 32, no. 3, pp.509–517, May/Jun. 1996.

[17] C. Newton and M. Summer, "Novel technique for maintaining balanced internal DC link voltages in diode-clamped five-level inverters," *Proc. Inst. Elect. Eng.—Elect. Power Appl.*, vol. 146, no. 3, pp. 341–349, May 1999.

AUTHORS PROFILE

A. Purna Chandra Rao received the B.E (Electrical and Electronics Engineering) degree From Andhra University, Visakhapatnam, India, M.Tech degree from Jawaharlal Nehru Technological University, Anantapur, India in 1998 and 2004 .He is currently working as an Associate Professor in the Dept. of Electrical and Electronic Engineering, at PVPSIT, Vijayawada, Andhra Pradesh. His area of interest is Power Electronics, and Electrical Drives.

Y. P. Obulesu received his B.E degree in Electrical Engineering from Andhra University, Visakhapatnam, India, M.Tech degree from Indian Institute of Technology, Kharagpur, India, in 1996 and 1998. He received his PhD degree from Jawaharlal Nehru Technological University, Hyderabad, in 2006. He has published several National and International Journals and Conferences. His area of interest is the simulation and design of power electronics systems, DSP controllers, fuzzy logic and neural network application to power electronics and drives.

Ch. Sai Babu received the B.E from Andhra University (Electrical & Electronics Engineering), M.Tech in Electrical Machines and Industrial Drives from REC, Warangal And PhD from JNTU, Hyderabad. Currently he is working as a Professor in Dept. of EEE & Director- Academic & Planning in JNTUK, Kakinada. He has published several National and International Journals and Conferences. His area of interest is Power Electronics and Drives, Power System Reliability, HVDC Converter Reliability, Optimization of Electrical Systems and Real Time Energy Management